11.0 Introduction

Differential amplifier or *diff-amp* is a multi-transistor amplifier. It is the fundamental building block of analog circuit. It is virtually formed the differential amplifier of the input part of an operational amplifier. It is used to provide high voltage gain and high common mode rejection ratio. It has other characteristics such as very high input impedance, very low offset voltage and very low input bias current.

Differential amplifier can operate in two modes namely common mode and differential mode. Each type will have its output response illustrated in Fig. 11.1. Common mode type would result zero output and differential mode type would result high output. This shall mean the amplifier has high common mode rejection ratio.

Figure 11.1: Differential amplifier shows differential inputs and common-mode inputs
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If two input voltage are equal, the differential amplifier gives output voltage of almost zero volt. If two input voltages are not equal, the differential amplifier gives a high output voltage.

Let’s define differential input voltage $V_{\text{in}(d)}$ as $V_{\text{in}(d)} = V_{\text{in}1} - V_{\text{in}2}$ and common-mode input voltage $V_{\text{in}(c)} = \frac{V_{\text{in}1} + V_{\text{in}2}}{2}$. From these equations, input voltage one and two are respectively equal to

$$V_{\text{in}1} = V_{\text{in}(c)} + \frac{V_{\text{in}(d)}}{2} \quad (11.1)$$

and

$$V_{\text{in}2} = V_{\text{in}(c)} - \frac{V_{\text{in}(d)}}{2} \quad (11.2)$$

The input voltage represented by common-mode voltage and differential voltage is shown in Fig. 11.2.

![Diagram of differential amplifier input voltages](image)

**Figure 11.2**: Small differential and common-mode inputs of a differential amplifier

Let $V_{\text{out}1}$ be the output voltage due to input voltage $V_{\text{in}1}$ and $V_{\text{out}2}$ be the output voltage due to $V_{\text{in}2}$. The differential-mode output voltage $V_{\text{out}(d)}$ be defined as $V_{\text{out}(d)} = V_{\text{out}1} - V_{\text{out}2}$ and common-mode output is defined $V_{\text{out}(c)} = \frac{V_{\text{out}1} + V_{\text{out}2}}{2}$. Combining these equations yield $V_{\text{out}1}$ as $V_{\text{out}2}$ respectively as equal to

$$V_{\text{out}1} = V_{\text{out}(c)} + \frac{V_{\text{out}(d)}}{2} \quad (11.3)$$
and

\[ V_{\text{out}2} = V_{\text{out}(c)} - \frac{V_{\text{out}(d)}}{2} \]  

(11.4)

Let \( A_{V1} = \frac{V_{\text{out}1}}{V_{\text{in}1}} \) be the gain of differential amplifier due to input \( V_{\text{in}1} \) only and \( A_{V2} = \frac{V_{\text{out}2}}{V_{\text{in}2}} \) due to input \( V_{\text{in}2} \) only. Then from superposition theorem, the output voltage \( V_{\text{out}} \) is equal to \( V_{\text{out}} = A_{V1} V_{\text{in}1} + A_{V2} V_{\text{in}2} \). After substituting \( V_{\text{in}1} \) and \( V_{\text{in}2} \) from equation (11.1) and (11.2), the output voltage \( V_{\text{out}} \) is equal to

\[ V_{\text{out}} = A_{V1} \left( V_{\text{in}(c)} + \frac{V_{\text{in}(d)}}{2} \right) + A_{V2} \left( V_{\text{in}(c)} - \frac{V_{\text{in}(d)}}{2} \right) \]  

(11.5)

Equation (11.5) is also equal to \( V_{\text{out}} = A_{V(\text{dm})} V_{\text{in}(d)} + A_{V(\text{cm})} V_{\text{in}(c)} \), where the differential voltage gain is \( A_{V(\text{dm})} = (A_{V1} - A_{V2})/2 \) and common-mode voltage gain is \( A_{V(\text{cm})} = (A_{V1} + A_{V2}) \).

The ability of a differential amplifier to reject common-mode signal depends on its common-mode rejection ratio CMRR, which is defined as

\[ \text{CMRR} = \left| \frac{A_{V(\text{dm})}}{A_{V(\text{cm})}} \right| \]  

(11.6)

From \( V_{\text{out}} = A_{V(\text{dm})} V_{\text{in}(d)} + A_{V(\text{cm})} V_{\text{in}(c)} \), output voltage \( V_{\text{out}} \) is equal to

\[ V_{\text{out}} = A_{V(\text{dm})} \left( V_{\text{in}(d)} + \frac{1}{\text{CMRR}} V_{\text{in}(c)} \right) \]  

(11.7)

Equation (11.7) clearly indicates that for large CMRR value, the effect of common-mode input is not significant to the output voltage.

**Example 11.1**

A differential amplifier shown in figure below has differential gain of 2,500 and a CMRR of 30,000. In part A of the figure, a single-ended input of signal 500µV rms is applied. At the same time a 1V, 50Hz interference signal appears on both inputs as a result of radiated pick-up from ac power system.

In part B of the figure, differential input signal of 500µV rms each is applied to the inputs. The common-mode interference is the same as in part A.
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1. Determine the common-mode gain.
2. Express CMRR in dB.
3. Determine the rms output signal for part A and B.
4. Determine the rms interface voltage on the output.

Solution
1. The common-mode gain $V_{cm} = A_{V(dm)}/\text{CMRR} = 2,500/30,000 = 0.083$.
2. CMRR = 30,000. Also $20\log(30,000) = 89.5\text{dB}$.
3. The difference input for part A is $500\mu\text{V} - 0\text{V} = 500\mu\text{V}$.
   Thus, the rms output is $A_{V(d)} \times 500\mu\text{V} = 2,500 \times 500\mu\text{V} = 1.25\text{Vrms}$
   The difference input for part B is $500\mu\text{V} - (-500\mu\text{V}) = 1\text{mV}$
   Thus, the rms output is $A_{V(d)} \times 1\text{mV} = 2,500 \times 1\text{mV} = 2.5\text{Vrms}$.
4. Since the common-mode gain $A_{cm}$ is 0.083 (from answer 1), then output voltage of interface from 1V 50Hz ac pick-up is $A_{cm} \times 1\text{V} = 0.083\text{V}$.

11.1 Bipolar Junction Transistor Differential Amplifier

Consider an emitter coupled bipolar junction transistor differential amplifier shown in Fig. 11.3. Assuming that the physical parameters of transistor $Q_1$ and $Q_2$ are closed to identical. With the modern fabrication technique and fabricating the transistor $Q_1$ and $Q_2$ in close approximation in the same wafer slide, close to identical physical parameters for both transistors are achievable.
11.1.1 dc Characteristics

Using Kirchhoff’s voltage law, the voltage at emitter $V_{E1}$ and $V_{E2}$, of the amplifier is $V_{in1} - V_{BE1} = V_{in2} - V_{BE2}$. From the theory of semiconductor physics, the collector current $I_C$ of a bipolar transistor is equal to $I_C = I_s \exp(V_{BE} / V_T) - 1$, where $I_s$ is the reverse saturation current, which is design dependent. $V_T$ is the thermal voltage, which has value approximately equal to 25.0mV at temperature 300K. Under normal operating conditions the term $\exp(V_{BE}/V_T) >> 1$, thus, the base-to-emitter voltage $V_{BE}$ is equal to $V_{BE} = V_T \ln\left(\frac{I_C}{I_s}\right)$. The differential input voltage $V_{in(d)} = (V_{in1} - V_{in2})$ shall then be equal to

$$V_{in(d)} = V_T \ln\left(\frac{I_{C1}}{I_{S1}} \cdot \frac{I_{S2}}{I_{C2}}\right) \tag{11.8}$$

For identical transistor pair reverse saturation current is $I_{S1} = I_{S2}$ and $V_{in(d)} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$. The ratio of collector current of transistor $Q_1$ and transistor $Q_2$ is equal to
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\[ \frac{I_{C1}}{I_{C2}} = \exp \left( \frac{V_{\text{in(d)}}}{V_T} \right) \]  

(11.9)

The emitter current is \( I_E = I_{E1} + I_{E2} \), which is also equal to \( I_E = \frac{I_{C1} + I_{C2}}{\alpha} \). Using this equation and equation (11.9), the collector current \( I_{C1} \) and \( I_{C2} \) of the transistor are separately derived shown in equation (11.10) and (11.11).

\[ I_{C1} = \frac{\alpha I_E}{1 + \exp \left( -\frac{V_{\text{in(d)}}}{V_T} \right)} \]  

(11.10)

\[ I_{C2} = \frac{\alpha I_E}{1 + \exp \left( \frac{V_{\text{in(d)}}}{V_T} \right)} \]  

(11.11)

The current transfer characteristic curve showing the plot of collector current of transistor \( Q_1 \) and \( Q_2 \) versus the differential input voltage \( V_{\text{in(d)}} \) is shown in Fig. 11.4.

Figure 11.4: The current transfer characteristic curve of a bipolar junction transistor differential amplifier

From the characteristic curve, once can notice that for several \( V_T \) values such as \( V_{\text{in(d)}} > 4V_T \), either \( I_{C1} \gg I_{C2} \) or \( I_{C1} \ll I_{C2} \) shall be obtained. For \( V_{\text{in(d)}} < 2V_T \), the collector current is almost linear.
At the output side, the output voltage are \( V_{\text{out}1} = V_{CC} - I_{C1}R_C \) and \( V_{\text{out}2} = V_{CC} - I_{C2}R_C \) respectively. The differential output voltage \( V_{\text{out}(d)} \) shall be \( V_{\text{out}(d)} = R_C(I_{C2} - I_{C1}) \). The differential output voltage \( V_{\text{out}(d)} \) also equal to

\[
V_{\text{out}(d)} = \alpha|E|E_\text{R}_C \left( \frac{1}{1 + \exp\left(\frac{V_{\text{in}(d)}}{V_T}\right)} - \frac{1}{1 + \exp\left(-\frac{V_{\text{in}(d)}}{V_T}\right)} \right)
\]

(11.12)

This equation is also equal to \( V_{\text{out}(d)} = \alpha|E|E_\text{R}_C \tanh\left(\frac{-V_{\text{in}(d)}}{2V_T}\right) \) since \( I_{C2} = 1/\left(1 + \exp(V_{\text{in}(d)}/V_T)\right) = \exp(-V_{\text{in}(d)}/2V_T)/(\exp(-V_{\text{in}(d)}/2V_T) + \exp(V_{\text{in}(d)}/2V_T) \) and \( I_{C1} = 1/\left(1 + \exp(-V_{\text{in}(d)}/V_T)\right) = \exp(V_{\text{in}(d)}/2V_T)/(\exp(V_{\text{in}(d)}/2V_T) + \exp(-V_{\text{in}(d)}/2V_T) \). The transfer characteristic of the output shall be as shown in Fig. 11.5.

From the analysis, one can see that to increase the range of input voltage so that it has more linear operating region, a separate emitter resistor which is termed as emitter-degeneration resistor, can be added to each transistor instead of sharing emitter resistor. This is because emitter current of each transistor will be double instead of half. This configuration will also improve the bandwidth of the amplifier.

### 11.1.2 Differential Mode

The differential input circuit of the amplifier is shown in Fig. 11.6.
Assuming identical transistor, the increase of emitter voltage by $V_{in1}$ i.e $V_{in(d)/2}$ is compensated by the decrease of same value of emitter voltage by $V_{in2}$ i.e. $-V_{in(d)/2}$. Thus, the voltage at emitter $E_1$ and $E_2$ remain unchange. Thus, the emitter current $I_e$ is approximately zero. As the result the potential at emitter is regards as same potential as ground level and $R_E$ is treated as short.

Based on the analysis, the ac differential input circuit of the amplifier can be split into two half circuits as one is shown in Fig. 11.7.

**Figure 11.6:** Differential input circuit of an emitter coupled BJT differential amplifier

**Figure 11.7:** ac differential mode half circuit of an emitter coupled BJT differential amplifier
The corresponding ac circuit of the half circuit amplifier is shown in Fig. 11.8.

![Diagram of ac circuit of circuit shown in Fig. 11.7](image)

**Figure 11.8:** ac circuit of circuit shown in Fig. 11.7

The output voltage is equal to

\[
\frac{V_{\text{out}(d)}}{2} = -g_m (R_C \parallel r_o) \frac{V_{\text{in}(d)}}{2}
\]

(11.13)

Thus, the differential-mode gain \( A_{V(\text{dm})} \) is equal to

\[
A_{V(\text{dm})} = \frac{V_{\text{out}(d)}}{V_{\text{in}(d)}} = -g_m (R_C \parallel r_o)
\]

(11.14)

The differential input impedance \( R_{\text{in}(d)} \) can be obtained from equation \( V_{\text{in}(d)}/2 = i_{b1} r_\pi \). Thus, the differential input impedance is equal to

\[
R_{\text{in}(d)} = 2r_\pi
\]

(11.15)

The differential output impedance \( R_{\text{out}(\text{dm})} \) can be obtained from equation \( V_{\text{out}(\text{dm})}/2 = i_C (r_o||R_C) \). Thus, the differential output impedance \( R_{\text{out}(\text{dm})} \) is equal to

\[
R_{\text{out}(d)} = 2(r_o||R_C)
\]

(11.16)

**11.1.2 Common Mode**

The common input circuit of the amplifier is shown in Fig. 11.9 and its corresponding half circuit is shown in Fig. 11.10. Since emitter voltage at emitter \( E_1 \) and \( E_2 \) is changing, therefore, the emitter resistance of the half circuit should be \( 2R_E \) instead of \( R_E \) after splitting into two half circuits.
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Figure 11.9: Common input circuit of an emitter coupled BJT differential amplifier

Figure 11.10: ac common mode half circuit of an emitter coupled BJT differential amplifier

The corresponding ac circuit of the half circuit amplifier is shown in Fig. 11.11.
At input side, \( V_{\text{in}(c)} = i_{b1}r_\pi + i_{b1}(\beta+1)2R_E \). Thus, the common-mode input impedance \( R_{\text{in}(c)} \) is equal to

\[
R_{\text{in}(c)} = [r_\pi + (\beta +1)2R_E] \quad (11.17)
\]

The common-mode output impedance \( R_{\text{out}(c)} \) is equal to \((R_C\|r_o)\).

The output common-mode voltage \( V_{\text{out}(c)} = -\beta i_{b1}(R_C\|r_o) \). The common-mode gain \( A_{V_{\text{cm}}} \) is equal to

\[
A_{V_{\text{cm}}} = \frac{V_{\text{out}(c)}}{V_{\text{in}(c)}} = -\frac{\beta i_{b1}(R_C\|r_o)}{i_{b1}r_\pi + 2R_E(\beta +1)} = -\frac{g_mR_C\|r_o}{1 + 2g_mR_E(1+1/\beta)} \quad (11.18)
\]

### 11.1.3 Common Mode Rejection Ratio

The common-mode rejection ratio of the emitter coupled BJT differential amplifier is equal to \( \text{CMRR} = A_{V_{\text{dm}}} / A_{V_{\text{cm}}} \). Thus from equation (11.14) and (11.18), common-mode rejection ration is

\[
\text{CMRR} = \frac{-g_m(R_C\|r_o)}{-g_m(R_C\|r_o)} \cdot [1 + 2g_mR_E(1+1/\beta)] = [1 + 2g_mR_E(1+1/\beta)]
\]

\( (11.19) \)

For large \( \beta \) value, the common rejection ratio is approximately equal to \( \text{CMRR} = [1 + 2g_mR_E] \). Thus, one can see for high common rejection ratio CMRR,
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the differential amplifier should be designed with high emitter resistance and high transconductance values.

11.2 JFET Differential Amplifier

A JFET differential amplifier is shown in Fig. 11.12 and its ac equivalent circuit is shown in Fig. 11.4. Since JFET has very high impedance, it satisfies the high impedance and low input bias current requirements for the differential amplifier. Theoretically, the JFETs M₁ and M₂ should have same physical parameters. This can be achieved via modern fabrication technique. This shall also mean that close to zero offset voltage is also achievable.

![Figure 11.12: A JFET differential amplifier](image)

11.2.1 dc Characteristics

Using Kirchhoff’s voltage law, the voltage at source of the amplifier is \(-V_{\text{in}1} + V_{\text{GS}1} + V_{\text{in}2} - V_{\text{GS}2} = 0\). Drain current of JFET is \(I_D = I_{\text{DSS}} \left(1 - \frac{V_{\text{GS}}}{V_{\text{GSOFF}}}\right)^2\).

Therefore, \(\frac{V_{\text{GS}1}}{V_{\text{GSOFF}}} = 1 - \sqrt{\frac{I_{\text{D1}}}{I_{\text{DSS}}}}\) and \(\frac{V_{\text{GS}2}}{V_{\text{GSOFF}}} = 1 - \sqrt{\frac{I_{\text{D2}}}{I_{\text{DSS}}}}\). Since \(-V_{\text{in}1} + V_{\text{in}2} = V_{\text{GS}2} - \)
\[ V_{G_{\text{S1}}}, \ V_{\text{in1}} - V_{\text{in2}} = V_{G_{\text{S(off)}}} \sqrt{\frac{I_{D2}}{I_{DSS}}} - V_{G_{\text{S(off)}}} \sqrt{\frac{I_{D1}}{I_{DSS}}}. \]

Since \( V_{\text{in1}} - V_{\text{in2}} = V_{\text{in(d)}} \), this equation becomes

\[ \frac{V_{\text{in(d)}}}{V_{G_{\text{S(off)}}}} = \sqrt{\frac{I_{D2}}{I_{DSS}}} - \sqrt{\frac{I_{D1}}{I_{DSS}}} \]  \hspace{1cm} (11.20)

\( I_S \) current is equal to the sum of \( I_{D1} \) and \( I_{D2} \). Thus, \( I_S = I_{D1} + I_{D2} \). Substituting this equation into equation (11.20) and solve the resultant quadratic, it yields drain current one and two, which are

\[ I_{D1} = \frac{I_S}{2} + \frac{I_S}{2} \left( \frac{V_{\text{in(d)}}}{V_{G_{\text{S(off)}}}} \right) \left[ 2 \left( \frac{I_{DSS}}{I_S} \right) - \left( \frac{V_{\text{in(d)}}}{V_{G_{\text{S(off)}}}} \right)^2 \left( \frac{I_{DSS}}{I_S} \right)^2 \right]^{1/2} \]  \hspace{1cm} (11.21)

and

\[ I_{D2} = \frac{I_S}{2} - \frac{I_S}{2} \left( \frac{V_{\text{in(d)}}}{V_{G_{\text{S(off)}}}} \right) \left[ 2 \left( \frac{I_{DSS}}{I_S} \right) - \left( \frac{V_{\text{in(d)}}}{V_{G_{\text{S(off)}}}} \right)^2 \left( \frac{I_{DSS}}{I_S} \right)^2 \right]^{1/2} \]  \hspace{1cm} (11.22)

The equation for drain current is only true for sum of the drain currents less than \( I_{DSS} \) current. The plot of drain current versus input differential voltage \( V_{\text{in(d)}} \) is shown in Fig. 11.13.
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The output voltage $V_{out1}$ and $V_{out2}$ are respectively equal to $V_{DD} - I_{D1}R_D$ and $V_{DD} - I_{D2}R_D$. The differential output voltage $V_{out(d)} = V_{out1} - V_{out2} = R_D(I_{D2} - I_{D1})$. Substituting equation (11.21) and (11.22) yields the differential output voltage $V_{out(d)}$ as

$$V_{out(d)} = -\frac{I_S R_D}{V_{GS(off)}} V_{m(d)} \left[ 2 \left( \frac{I_{DSS}}{I_S} \right) - \left( \frac{V_{m(d)}}{V_{GS(off)}} \right) \left( \frac{I_{DSS}}{I_S} \right)^2 \right]^{1/2} \quad (11.23)$$

11.2.1 Differential Mode

The differential input of the JFET differential amplifier can be analyzed like the way how the analysis is done for BJT counterpart. The half circuit of the amplifier is shown in Fig. 11.14.

![Figure 11.14: ac differential mode half circuit of a JFET differential amplifier](image)

The corresponding ac circuit of the half circuit amplifier is shown in Fig. 11.15.

![Figure 11.15: ac circuit of circuit shown in Fig. 11.14](image)
The output voltage \( \frac{V_{\text{out(d)}}}{2} \) is equal to

\[
\frac{V_{\text{out(d)}}}{2} = -g_m (R_D \parallel r_o) \frac{V_{\text{in(d)}}}{2}
\] (11.24)

Thus, the differential-mode gain \( A_{V_{\text{dm}}} \) is equal to

\[
A_{V_{\text{dm}}} = \frac{V_{\text{out(d)}}}{V_{\text{in(d)}}} = -g_m (R_D \parallel r_o)
\] (11.25)

Normal \( R_D << r_o \) then the differential-mode gain \( A_{V_{\text{dm}}} \) is

\[
A_{V_{\text{dm}}} = \frac{V_{\text{out(d)}}}{V_{\text{in(d)}}} = -g_m R_D.
\]

### 11.2.2 Common Mode

The common input circuit of the amplifier is shown in Fig. 11.16 and its corresponding half circuit is shown in Fig. 11.17. Since source voltage at emitter \( S_1 \) and \( S_2 \) is changing, therefore, the emitter resistance of the half circuit should be \( 2R_D \) instead of \( R_D \) after splitting into two half circuits.

![Diagram of Common input circuit of a JFET differential amplifier](image)

**Figure 11.16:** Common input circuit of a JFET differential amplifier

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Figure 11.17: ac common mode half circuit of a JFET differential amplifier

The corresponding ac circuit of the half circuit amplifier is shown in Fig. 11.18.

![Circuit Diagram](image)

Figure 11.18: ac circuit of circuit shown in Fig. 11.17

At input side, common-mode input voltage is $V_{\text{in(c)}} = V_{gs1} + g_m V_{gs1} 2R_s$. Thus, the common-mode input impedance $R_{\text{in(c)}} = \frac{V_{\text{in(c)}}}{I_{\text{gate}}}$ is equal to

$$R_{\text{in(c)}} = \frac{V_{gs} + g_m 2V_{gs} R_s}{I_{\text{gate}}} = R_{\text{in(gate)}}(1 + 2g_m R_s) \quad (11.17)$$
where $V_{gs}/I_{\text{gate}} = R_{\text{in(gate)}}$. Depending on the value of $R_{\text{in(gate)}}$ that can be a infinite value for very small $I_{\text{gate}}$ current.

The output common-mode voltage $V_{\text{out(c)}} = -g_m V_{gs1}(R_D || r_o)$. The common-mode gain $A_{V(cm)} = \frac{V_{\text{out(d)}}}{V_{\text{in(d)}}}$ is equal to

$$A_{V(cm)} = -\frac{g_m V_{gs1}(R_D || r_o)}{V_{gs1} + 2g_m V_{gs1} R_S} = -\frac{g_m (R_D || r_o)}{1 + 2g_m R_S}$$

(11.26)

### 11.2.3 Common Mode Rejection Ratio

The common-mode rejection ratio of the JFET differential amplifier is equal to $CMRR = A_{V(dm)}/A_{V(cm)}$. Thus from equation (11.25) and (11.26), common-mode rejection ratio is

$$CMRR = \frac{-g_m (R_D || r_o)}{-g_m (R_D || r_o)} [1 + 2g_m R_S] = [1 + 2g_m R_S]$$

(11.27)

### 11.3 MOSFET Differential Amplifier

A JFET differential amplifier is shown in Fig. 11.19. Using Kirchhoff’s voltage law, the voltage at source of the amplifier is $-V_{in1} + V_{GS1} + V_{in2} - V_{GS2} = 0$. Drain current of MOSFET is $I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_t)^2 = K_n (V_{GS} - V_t)^2$, where $K_n = \frac{\mu_n C_{ox} W}{2L}$. This implies that $V_{GS} = \frac{I_D}{K} + V_t$. From equation $-V_{in1} + V_{GS1} + V_{in2} - V_{GS2} = 0$. The differential input voltage $V_{in(d)}$ is

$$V_{in(d)} = V_{in1} - V_{in2} = \frac{I_{D2}}{K} + V_t - \frac{I_{D1}}{K} - V_t = \frac{I_{D2}}{K} - \frac{I_{D1}}{K}$$

(11.28)

From Kirchhoff’s current law, $I_S = I_{D1} + I_{D2}$ and substituting $V_{in(d)}$. The drain currents are found to be
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\[ I_{D1} = \frac{I_s}{2} + \sqrt{2K_nI_S} \left( \frac{V_{in(d)}}{2} \right) \left[ 1 - \frac{(V_{in(d)}/2)^2}{(I_s/2K_n)} \right]^{1/2} \]  \hspace{1cm} (11.29)

and

\[ I_{D1} = \frac{I_s}{2} - \sqrt{2K_nI_S} \left( \frac{V_{in(d)}}{2} \right) \left[ 1 - \frac{(V_{in(d)}/2)^2}{(I_s/2K_n)} \right]^{1/2} \]  \hspace{1cm} (11.30)

Employing the method used in JFET differential amplifier analysis, the common-mode gain \( A_{V(cm)} \) and differential-mode gain \( A_{V(dm)} \) are found to be

\[ V_{out(d)} = -R_D \left( \frac{K_nI_s}{2} \right)^{1/2} V_{in(d)} \]  \hspace{1cm} (11.31)

Figure 11.19: A MOSFET differential amplifier
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\[ A_{V(cm)} = \frac{-g_m R_D}{1 + 2g_m R_s} \] and \[ A_{V(dm)} = A_{V(dm)} = g_m R_D \] respectively. Subsequently, the common-mode rejection ratio CMRR is found to be \[ CMRR = \left[ 1 + 2g_m R_s \right]. \]

### 11.3.1 Active Load MOSFET Differential Amplifier

Let’s consider an active load MOSFET differential amplifier shown in Fig. 11.20. MOSFET M1 and M2 formed the differential pair. They have same design parameters. MOSFET M5 is current sink, which provides the bias current to the amplifier. MOSFET M3 and M4 form a current mirror, which is assumed to have same design parameters.

From Kirchhoff’s current law, current \( I_{D5} \) is equal to the sum of current \( I_{D1} \) and \( I_{D2} \). If the input voltage \( V_{in1} \) and \( V_{in2} \) are equal then current \( I_{D1} = I_{D2} = I_{D3} = I_{D4} \). This shall mean the output current \( I_{out} \) is equal to zero. Thus, output voltage \( V_{out} \) is equal to zero.

If the input voltage \( V_{in1} \) is greater than \( V_{in2} \), which \( V_{in1} > V_{in2} \), then current \( I_{D1}, I_{D3}, \) and \( I_{D4} \) are equal. This shall mean current \( I_{D1} \) is greater than \( I_{D2} \). Therefore, at output node current is \( I_{D4} = I_{D2} + I_{out} \). This result implies that the output voltage is a positive value.

If the input voltage \( V_{in2} \) is greater than \( V_{in1} \), which \( V_{in2} > V_{in1} \), then current \( I_{D1}, I_{D3}, \) and \( I_{D4} \) are equal. This shall mean current \( I_{D1} \) is less than \( I_{D2} \). This implies that current \( I_{D2} \) is equal to the sum of current \( I_{D4} \) and \( I_{out} \), i.e. \( I_{D2} = I_{D4} + I_{out} \).

The differential input voltage is \( V_{in(d)} = (V_{in1} - V_{in2}) \). For each input of the differential pair would see a change of \( (V_{in1} - V_{in2})/2 = V_{in(d)}/2 \). Thus, a change in input \( V_{in(d)}/2 \) will result a change of \( g_m V_{in(d)}/2 \) for the drain current of MOSFET M1 and M2. The ac equivalent circuit of output side is shown in Fig. 11.21.

The differential voltage gain \( A_{V(dm)} \) of the differential amplifier is found to be

\[ A_{V(dm)} = \frac{V_{out}}{V_{m2} - V_{m1}} = \frac{1}{2} \left( g_{m2} + g_{m4} \right) r_{D4} || R_L \] (11.32)
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Figure 11.20: An active load MOSFET differential amplifier

From Kirchhoff’s voltage law, output voltage is
\[ V_{\text{out}} = - \left( g_{m2} V_{\text{in(d)}}/2 + g_{m4} V_{\text{in(d)}}/2 \right) \left( r_{o1} || r_{o4} || R_L \right). \]

Therefore, the differential voltage gain \( A_{V(\text{dm})} \) is
\[ A_{V(\text{dm})} = \frac{V_{\text{out}}}{V_{\text{in2}} - V_{\text{in1}}} = -\frac{1}{2} \left( g_{m2} + g_{m4} \right) \left( r_{o2} || r_{o4} || R_L \right). \]

In normal circumstance transcondctance \( g_{m2} \) is equal to transconductance \( g_{m4} \). i.e. \( g_{m2} = g_{m4} \). Thus, the differential gain is \( A_{V(\text{dm})} = -g_{m2} \left( r_{o2} || r_{o4} || R_L \right). \) Since the output impedance of the MOSFET \( r_{o4} \) and \( r_{o2} \) are large, it can be assumed that they are equal. If the load \( R_L \) is not connected then the differential gain equation \( A_{V(\text{dm})} = -\frac{g_{m2}}{2} r_o \), where \( r_{o4} = r_{o2} = r_o \). The equation demonstrates that the differential gain is a large constant for a given MOSFET in active load configuration.
11.4 BiCMOS Differential Amplifier

The differential mode gain of a BJT differential amplifier is equal to $A_{V(dm)} = -g_m r_o$. It is also equal to $A_{V(dm)} = -\frac{I_C}{2V_T} \cdot \frac{2V_A}{I_C} = -\frac{V_A}{V_T}$. This result shows that the gain is a constant value. For a typical Early voltage $V_A$ of 50V and thermal voltage $V_T$ of 25mV, the gain is $-2,000V/V$. Thus, lowering the collector current $I_C$ will improve input impedance but reducing $g_m$, thus, sacrificing bandwidth because the unity gain frequency $f_T$ of BJT is $\frac{g_m}{2\pi(C_{in} + C_x)}$. The input impedance of the BJT is equal to $r_x = \frac{\beta}{g_m} = \frac{V_x}{I_c}$.

The differential mode gain $A_{V(dm)}$ of a MOSFET differential amplifier is equal to $A_{V(dm)} = -g_m r_o = -\frac{2K}{I_D} \cdot \frac{2V_M}{I_D} = -2V_M \sqrt{\frac{2K}{I_D}}$, which shall mean gain is inversely proportional to $\sqrt{I_D}$. Since the thermal voltage $V_M$ of MOSFET is much lower than the thermal voltage of BJT differential amplifier, the differential gain $A_{V(dm)}$ of BJT is much higher than differential gain of MOSFET differential amplifier. If drain current $I_D$ is lower, the bandwidth of the amplifier reduces because the transconductance $g_m$ is proportional to $\sqrt{I_D}$ and the unity gain frequency $f_T$ is proportional to transconductance $g_m$. The input impedance of the MOSFET has infinite value. Combining the high gain of BJT and infinite impedance of MOSFET will lead to BiCMOS differential amplifier design that
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can be a basic configuration, cascade configuration, active load configuration, etc. The circuit of active load BiCMOS differential amplifier is shown in Fig. 11.22.

\[ A_{V(dm)} = \frac{V_{out}}{V_{in2} - V_{in1}} = -\frac{1}{2} (g_{m2} + g_{m4})(r_{o2} \parallel r_{o4} \parallel R_L) \]  \hspace{1cm} (11.33)

whereby  \( g_{m2} = \frac{2V_{M}}{I_{D5}}, \quad g_{m4} = \frac{2V_{M}}{I_{D5}}, \quad r_{o4} = \frac{2V_{M}}{I_{D5}}, \) and  \( r_{o2} = \frac{2V_{M}}{I_{D5}}. \) In normal circumstance  \( g_{m2} = g_{m4}. \) Thus, the differential gain is  \( A_{V(dm)} = \frac{V_{out}}{V_{in2} - V_{in1}} = -g_{m2} (r_{o2} \parallel r_{o4} \parallel R_L). \)

**Example 11.2**
A BiCMOS differential amplifier as shown in Fig. 11.21 has $I_{D5} = 10\mu A$, identical BJT with $V_A = 50V$ and $\beta = 40$, identical MOSFET with $V_M = 20V$, $K = 25\mu A/V^2$, $W = 30\mu m$, $L = 10\mu m$, $V_{GS} = 1.0V$, $V_{DD} = 10V$ and $V_{SS} = 10V$. Determine the differential gain of the amplifier without the load $R_L$ and $V_{bias}$ voltage.

**Solution**

The output impedance of the BJT is $2V_A/I_{D5} = 2 \times 50/10\mu A = 4M\Omega$.

The output impedance of the MOSFET is $2V_M/I_{D5} = 2 \times 20/10\mu A = 10M\Omega$.

The overall output impedance $R_O$ of differential amplifier is $4M\Omega||10M\Omega = 2.86M\Omega$.

The transconductance $g_{m2}$ of MOSFET is $\sqrt{2KI_{D5}} = \sqrt{2 \times 25\mu A/V^2 \times 10\mu A} = 22.36\mu A/V$.

Thus, the differential voltage gain $A_{V(dm)}$ is $-g_{m2}R_O = - 22.36 \times 2.86M\Omega = - 63.9$.

The gate-to-source voltage of MOSFET $M_5$ is $1.5V$. The current $I_{D5}$ is $I_{D5} = \frac{C_{OX}\mu_n}{2}\left(\frac{W}{L}\right)(V_{GS} - V_m)^2 = 2.5 \times 10^{-5} \times 3/2(V_{GS} - 1.0)^2 = 10\mu A$. This implies that $V_{GS}$ is equal to $1.51V$.

Since $V_S = -10V$ and $V_{GS} = V_{bias} - V_S$, $V_{bias}$ is equal to $-8.49V$.

**11.5 Cascode Differential Amplifier**

Let’s discuss one type of cascade differential amplifier, which is bipolar junction transistor type.

Consider a BJT cascode differential amplifier shown in Fig. 11.23. This configuration is usually to improve the output resistance for the gain and frequency response. Transistor $Q_5$ and $Q_6$ are connected as common base amplifier.

The half circuit of the amplifier is shown in Fig. 11.24. The ac circuit of the half circuit amplifier is shown in Fig. 11.25.

From the ac circuit $r_{\pi 0}/(\beta+1)$ is parallel to $r_{o2}$ i.e. $r_{\pi 0}/(\beta+1) || r_{o2}$. All $r_{o2}$, $r_{o4}$, and $r_{o6}$ are the same because the collector current flows in them are the same $r_o$. The transconductance $g_{m2}$, $g_{m4}$, and $g_{m6}$ should be equal to $g_m$. 

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Figure 11.23: A BJT cascode differential amplifier
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Figure 11.24: Half circuit of a BJT cascade differential amplifier
The output voltage is equal to $V_{out} = -g_m V_{in(d)} (r_o \parallel R_L)$. Thus, the differential-mode gain is equal to $A_{V(dm)} = -g_m (r_o \parallel R_L)$.

Figure 11.25: ac circuit of the half circuit differential amplifier

11.6 Effect of Device Mismatch

An ideal BJT differential amplifier has identical transistor pair and bias resistors. This shall mean that if the differential input voltage $V_{in(d)}$ is zero then the differential output voltage $V_{out(d)}$ should be zero. In reality, there should have some mismatch in the bias resistor and the transistor pair should have offset difference.

The offset voltage of a differential amplifier $V_{os}$ is defined the input differential voltage $V_{in(d)}$ required to drive the output differential voltage $V_{out(d)}$ to zero voltage. From Fig. 11.2, the offset voltage $V_{os}$ shall be $V_{os} = V_{be1} - V_{be2}$, which is also equal to

$$V_{os} = V_T \ln \left( \frac{I_{C1}}{I_{S1}} \cdot \frac{I_{S2}}{I_{C2}} \right)$$  \hspace{1cm} (11.34)

Offset voltage can also be expressed as the change of collector resistance and reverse saturation current of the transistors in which it follows equation (11.35).
11.7 Frequency Response of Differential Amplifier

If the base resistor $R_B$ is added to the bipolar junction transistor differential amplifier circuit shown in Fig. 11.2, then the differential mode voltage gain $A_{v(dm)}$ shall be $A_{v(dm)} = -g_m R_C \frac{r_n}{r_n + R_B}$. From the earlier analysis of high frequency response of the common-emitter configuration, the differential mode voltage gain transfer function is $A_{v(dm)}(s) = \frac{-g_m R_C \frac{r_n}{r_n + R_B}}{1 + s \frac{R_B (C_m + C_\mu)}{R_C}} \left(1 + s \frac{R_C (C_\mu + C_{ce})}{R_B}ight)^{-1}$, where $C_M$ is Miller's capacitance, which is equal to $C_\mu (1 + g_m R_C)$ and $C_\mu$ is the collector-to-base capacitance. From the function, it shows there are two critical frequency $f_H$ and $f_{H1}$ determined by $\frac{1}{2\pi \| R_B (C_m + C_\mu) \|$} and $\frac{1}{2\pi \left[ R_B (C_\mu + C_{ce}) \right]}$. However, due to very small value of $C_{ce}$ and $C_\mu$, and small $R_C$, the critical frequency is extremely high, which can be infinite. Since there is no coupling capacitor in the circuit, the bandwidth different mode gain shall be from zero Hz frequency to $f_H$. The frequency response is shown in Fig. 11.26.

The frequency response for the common mode voltage gain of the amplifier can be analyzed using small signal equivalent half circuit shown in Fig. 11.27 and the emitter current source is replaced with a capacitor $C_o$ and a resistor $R_o$. 

\[
V_{os} = V_T \left( -\frac{\Delta R_C}{R_C} - \frac{\Delta I_S}{I_S} \right) \quad (11.35)
\]

where $\Delta R_C = R_{C1} - R_{C2}$, $\Delta I_S = I_{S1} - I_{S2}$, $R_c = \frac{R_{C1} + R_{C2}}{2}$, and $I_c = \frac{I_{S1} + I_{S2}}{2}$.
The common mode output voltage $V_{\text{out(c)}}$ is $-g_m V_\pi R_C$. At base-to-emitter loop, from Kirchhoff’s voltage law, it produces $V_{\text{in(c)}}(s) = V_\pi + \left( \frac{1}{2} \right) \left( \frac{R_B}{r_\pi} \right) + \frac{2 g_m V_\pi}{R_o \parallel \frac{1}{sC_o}}$. Substituting $V_\pi$ from $V_{\text{out(c)}}(s)$ equation, the common mode voltage gain $A_{V_{\text{cm}}}(s)$ shall be
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\[
A_{V(cm)}(s) = \frac{-g_m R_C (1 + s R_o C_o)}{(1 + R_B) (1 + s R_o C_o) + \frac{2(1 + \beta) R_o}{r_x}}
\]

The gain equation shows that there is a zero and a pole. From the zero, the critical frequency \( f_Z \) shall be \( 1/(2\pi R_o C_o) \). The zero also explains why \( C_o \) parallel with \( R_o \). At low frequency, \( C_o \) is a open circuit and the common signal see impedance \( R_o \). As frequency increase, the impedance \( C_o \) decreases and \( R_o \) becomes bypassed. Since the current source can has very high resistance \( R_o \) and small capacitance \( C_o \), the critical frequency can be very small. Soon the operating frequency is more than the critical frequency, the gain of the amplifier increases at the rate 20 dB/decade or 6 dB/octave. Figure 11.28 illustrates the frequency response.

![Frequency response of the common mode gain](image)

**Figure 11.28:** Frequency response of the common mode gain

From equation (11.36), the critical frequency of the pole is

\[
f_p = \frac{1}{2\pi R_{eq} C_o}
\]

where \( R_{eq} = \frac{R_o \left( 1 + \frac{R_B}{r_x} \right)}{1 + \frac{R_B}{r_x} + \frac{2(1 + \beta) R_o}{r_x}} \). The denominator of this resistance \( R_{eq} \) is very large due to \( (1 + \beta) R_o \) term. This shall mean that \( R_{eq} \) is very small. Therefore, the critical frequency is very high.
If the ratio of the frequency response for differential mode gain and common mode gain is plotted, then the frequency response of common mode rejection ratio shall be obtained and it is shown in Fig. 11.29.

Figure 11.29: Frequency response of the common mode rejection ratio
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Exercises

11.1. An active load emitter coupled BJT differential amplifier is shown in the Fig.

i. Draw differential half circuit for the amplifier.

ii. Show that the differential-mode gain $A_{V_{dm}} = -g_m (r_{o2} \parallel r_{o4} \parallel R_L)$.

iii. If $r_{o2} = r_{o4} = r_{o}$, prove that the differential-mode gain is equal to $A_{V_{dm}} = \frac{V_\Delta}{2V_T}$.

iv. Calculate the room temperature differential-mode gain of the amplifier if the Early voltage of the transistor is 80V and express the result in decibel.

v. Comment the result.

11.2. An $n$-channel MOSFET differential amplifier is shown below. Both MOSFETs have aspect ratio $W/L = 25\mu m/1.0\mu m$, $\mu_nC_{ox} = 50\mu A/V^2$, threshold voltage $V_T = 0.6V$, and $V_{DD} = 3.0V$. You may use equation $I_D = W\mu_nC_{ox} \left( V_{GS} - V_T \right)^2$ for calculation and assume both MOSFET's have same design parameters.
i. Prove that the common mode gain of the amplifier is 
\[ \frac{R_D}{2} \frac{1}{1/(2g_m) + R_S} \].

ii. What is the common mode input voltage \( V_{in1} = V_{in2} \) for the voltage drop across resistor \( R_S \) to be 0.6V?

iii. What should be the value of resistor \( R_S \) for maintaining 0.6V voltage drops across it?

11.3. An n-channel MOSFET differential amplifier is show below has common mode gain follow expression 
\[ \frac{R_D}{2} \frac{1}{1/(2g_m) + R_S} \]. Both MOSFETs have aspect ratio \( W/L = 25\mu m/1.0\mu m \), \( \mu_nC_{ox} = 50\mu A/V^2 \), threshold voltage \( V_T = 0.6V \), \( R_S = 600\Omega \), and \( V_{DD} = 3.0V \). You may use equation \( I_D = \frac{W\mu_nC_{ox} (V_{GS} - V_T)^2}{2L} \) for calculation and assume both MOSFET's have same design parameters.
i. Prove that the differential mode gain of the amplifier is \(-g_m R_D\).

ii. Derive the equation for transconductance \(g_m\).

iii. Derive the formula for the common rejection ratio for the amplifier. State a way to improve this parameter.

iv. Calculate the common rejection ratio of this amplifier and express the result in decibel.

11.4. The parameters of the emitter-coupled pair BJT differential amplifier are \(\beta = 100, R_E = 50 \, \text{k}\Omega, I_E = 1\, \text{mA}, V_{CC} = 15\, \text{V}, R_C = 10 \, \text{k}\Omega\).

i. Calculate the dc collector current of \(V_{in(d)} = 5\, \text{mV}\).

ii. Calculate the CMRR of the amplifier.

11.5. The design of JFET differential amplifier is shown in the Fig. with one input terminal is grounded. The dc biasing current \(I_S = 10\, \text{mA}, V_{DD} = -V_{SS} = 15\, \text{V}\). The JFETs are identical and have \(V_{GS(off)} = -4.0\, \text{V}\) and \(I_{DSS} = 20\, \text{mA}\). A small signal voltage of \(A_1 = -10\) is required. Calculate the design values of \(A_{V(dm)}\), \(A_{V(cm)}\), and CMRR.
11.6. Calculate the differential gain of the given MOSFET amplifier circuit shown in the in figure. Given that $V_{\text{bias}} = -3.5\text{V}$, $\mu_n C_{\text{ox}} = 5.2 \times 10^{-5} \text{A/V}^2$, $\mu_p C_{\text{ox}} = 2.1 \times 10^{-5} \text{A/V}^2$, $V_{\text{in}} = 0.7\text{V}$, $V_{\text{tp}} = -0.7\text{V}$, $(W/L)_{1,2} = 40$, $(W/L)_{3,4} = 20$, $(W/L)_5 = 40$, $(1/\lambda)_{1,2} = 0.01$, $(1/\lambda)_{3,4} = 0.02$, and $R_L = 5.0\text{k}\Omega$. 
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\[ \text{Bibliography} \]