Electrical Overstress Course

EOS Training Course

Dr. Lim Soo King
Dip Sc (Merit); B Sc (Hons); Dip Mgt (Dist)
M Sc; PhD; MIPM
Associate Professor
Universiti Tunku Abdul Rahman

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Objectives of the Course

- Understand the phenomena of EOS.
- Ability to set-up an effective EOS program for the organization.
- To improve the cost, quality, cycle time, and reliability.
- To reduce customer complaint.
- Reduce the wastage due to EOS.
Introduction
Outline of the Course

- Introduction.
- Theory of EOS.
- Characteristics of EOS.
- Miniaturization of device.
- Device structures.
- Causes of EOS.
Outline of the Course

- Failure mechanism of EOS.
- Theory of failure.
- EOS test methodology.
- EOS prevention
- Reference.
- JVC case study.
Introduction

- EOS is defined as electrical overstress.
- Semiconductor devices have a limited ability to sustain electrical overstress.
- The device susceptibility to EOS increases as the device is scaled down to submicron feature size.
- 37% for the IC failures can be attributed to ESD/EOS events.
World Revenue of Semiconductor

Bil $
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#### Roadmap of Device

<table>
<thead>
<tr>
<th>Year</th>
<th>99</th>
<th>02</th>
<th>05</th>
<th>08</th>
<th>11</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length (µm)</td>
<td>0.18</td>
<td>0.13</td>
<td>0.10</td>
<td>0.07</td>
<td>0.05</td>
<td>0.035</td>
</tr>
<tr>
<td>Equivalent oxide thickness (µm)</td>
<td>1.9 - 2.5</td>
<td>1.5 - 1.9</td>
<td>1.0 - 1.5</td>
<td>0.8 - 1.2</td>
<td>0.6 - 0.8</td>
<td>0.5 - 0.6</td>
</tr>
<tr>
<td>Transistor density (cm²)</td>
<td>6.6M</td>
<td>18 M</td>
<td>44 M</td>
<td>109 M</td>
<td>269 M</td>
<td>664 M</td>
</tr>
</tbody>
</table>
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Field Return Failure Mode

- Fab: 26%
- Assembly: 14%
- Electrical QA: 1%
- Good: 4%
- Ion: 3%
- Unknown: 15%
- ESD/EOS: 37%
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Theory of EOS
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Theory of EOS

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An EOS failure is typically catastrophic and causes irreparable damage to the device.

- ESD and EOS are interrelated. Device weaken by ESD would have EOS easily.
- It is the large scale ESD.
- The duration of EOS events ranges from milliseconds to seconds (typical > 50 µsec).
Characteristics of EOS
Characteristics of EOS

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Characteristics of EOS

- Time duration a few ns to a µs to resulting ESD.
- Time duration > 50 µs to < 100 µs causes junction punch through.
- Time duration > 100 µs causes melt metal, fused wire, and bond wire.
Miniaturization of Device
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Miniaturization of Device

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Miniaturization of Device

- The permissible critical field strength of expitaxial layer can be only 100V depending on thickness and doping level.
- Shallow junction depth.
- Junction breakdown voltage is usually around 20V.
Device Structure
CMOS output consist of \( p \)-channel and \( n \)-channel MOSFETs.
CMOS output consist of \( p \)-channel and \( n \)-channel MOSFET
Device Structure

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Device Structure

Power MOSFET device structure - BJT and diode parasitic components
Device Structure

IGBT device structure
Causes of EOS
Causes of EOS

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Causes of EOS

- Device designed with parasitic component which is the source of EOS.
- Bad fabrication control
  - Over etch.
  - Photo resist residue.
- Violation of design rule.
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Causes of EOS

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Causes of EOS

- No common ground test system and device.
  Inductive effect.
  Resistive effect.
- Improper shutdown of device
  Wrong power sequencing.
  Hot-plug the device.
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Causes of EOS

- Poor quality system.
  - Burn-in spike.
- Poor specifications.
- Wrong orientation.
- PCB signal integrity.
- Transient overshoot and undershoot controlled within absolute max. rating.
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Causes of EOS

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Causes of EOS

- Noisy power source
  - Transient spike.
  - 5 V part with a 2.5 V spike – 50% EOS.
  - 2.5 V part with a 2.5 V spike – 100% EOS.
  - 1.5 V part with a 2.5 V spike – 167% EOS.
Failure Mechanism of EOS
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Failure Mechanisms

- Thermal-Induced failure
  - Doping level.
  - Junction depth.
  - Device characteristic particularly dimension.

- Electro-migration
  - High electric field.
  - Migration of metal ion from high field to low field area.
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Failure Mechanisms

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Failure Mode

Bond wire fused
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Failure Mode

Junction Failure
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Failure Mode

Metalization Melt Failure
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Failure Mode

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Failure Mode

Secondary breakdown

Metallization burn
Diffusion damage

Diffusion damage
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Failure Mode

I/O resistor damage

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Failure Mode

Thermal EOS – base-emitter region
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Failure Mode

Thermal EOS – melt wires

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Failure Mode

Thermal EOS – latch-up

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Failure Mode

- Blown metal line
- Melt contact and bus
- Melt bond pad
Theory of Failure
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Theory of Failure

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High current density that melts aluminum metallization and blows gold/Al bond wire.
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Theory of Failure - Undershoot

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Theory of Failure - Undershoot

- Simultaneous switching causing current from package, wire to be greater than forward current of diode resulting net current flow in package parasitic resistive and inductive components.
- This would cause the device’s ground well below the system.
The voltage difference between power pin and device ground will be far exceeding its normal $V_{CC}$ voltage.

This would cause EOS.

The illustration is shown in next few foils.
Theory of Failure - Undershoot

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Theory of Failure - Undershoot
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Theory of Failure - Undershoot

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As illustrated in previous graph, overshoot would result the ground of the device being shifted upward.

The voltage across the device is less than $V_{CC}$.

Soft-bit would be resulted as a problem.
Theory of Failure – Latch-up

- This is true for CMOS and IGBT devices.
- It is caused by input voltage is greater than the power supply voltage by at least 0.7V.
- 0.7 V is the forward voltage $V_F$ of a diode.
- The $p$-channel MOSFET acts lateral $pnp$ transistor.
- The $n$-channel MOSFET act as vertical $npi$ transistor.
- These two transistors are connected as thyristor.
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Theory of Failure – Latch-up

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Theory of Failure – Latch-up

- This event creates tremendous increase of current that the power density would melt the Al metallization or blow wire.
- Unclean power supply voltage would cause latch-up.
- Noise input such as overshoot would cause latch-up.
- The illustration of latch-up is shown in the following foils.
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Theory of Failure – Latch-up
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Theory of Failure – Latch-up

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Theory of Failure – Latch-up

$V_{BE}$ of npn transistor $> 0.7V$, leakage current, latch-up occurs.
High electric field. Electro-migration forces metal ions to move downstream mainly along the grain structure.
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EOS Test Methodology
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EOS Test Methodology

- Purpose is to weed out the infant mortality failure due to fab, assembly, handling, etc.
- Applying HBM, MM, CDM, field induced model, floating induced model according to Mil-std-883 E method 3015.7.
- Burn-in or “dirty” burn-in according to Mil-std-38510.
- Final test.
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Bathtub Curve of Device

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EOS Prevention
EOS Prevention

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EOS Prevention

- Prevent power surge by using uninterrupted power supply.
- Power line of PCB should be designed not too close to prevent high induced voltage.
- Use isolation when necessary.
- Use capacitor filtering (0.01µF) connecting to the power supply of device.
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EOS Prevention

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EOS Prevention

- Measure the parasitic resistance and inductance of the device package to minimize voltage difference between device ground and system ground.
- Prevent hot-plug of device into or out of PCB or test socket.
- Prevent high tension inductive field such as from computer terminal.
- Use shielding technique to eliminate interference.
EOS Prevention

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References

- ESDA S20.20.
- DOD-HBK-263 B.
- Mil-std-1686A.
- 883 E method 3015.7.
- Mil-std- 38510.
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Q and A Session
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