9.0 Introduction

Counter is another class of sequential circuits that tally a series of input pulses which may be regular or irregular in nature. Counter can be divided into binary/non-binary and synchronous/asynchronous types.

In the chapter the design of counter using various types of flip-flop are discussed.

9.1 Types of Counter

Counter can be broadly divided into synchronous and asynchronous types. Synchronous counter has its flip-flops clocked at the same time, whilst asynchronous counter is not. The clock of the preceeding flip-flop of the asynchronous flip-flop is fed from the output of the previous flip-flop. Asynchronous counter suffers delay problem whilst, sychronous counter will not. Asynchornous oounter is also referred as ripple counter for the reason of delay feeding of the clock pulse from one flip-flop to another. Figure 9.1 and 9.2 respectively shown a modulus 4 synchronous and asynchronous counters. Modulus of a counter is defined as the number of unique states that a counter will sequence through.

Figure 9.1: A modulus 4 2-bit synchronous counter
9.2 Propagation Delay

We have mentioned in earlier in Chapter one that there is propagation delay when data is transmitted from one device to another due to capacitance of the device. The problem associated with propagation delay can be serious. We shall illustrate propagation delay with a 3-bit binary counter and its timing diagram shown in Fig. 9.3 and 9.4 respectively.
From the timing diagram, it shows there are propagation delays due to transition from clock pulse to output of flip-flop 0 $Q_0$, from output of flip-flop 0 $Q_0$ to output flip-flop 1 $Q_1$, and from output of flip-flop 1 $Q_1$ to output flip-flop 2 $Q_2$.

If the output $Q_1$ is AND’ed with output $\overline{Q_0}$, the ideal result i.e. the assumption of no propagation delay is shown in Fig. 9.5, whereas the result shown in Fig. 9.6 is different for the case where there is propagation delay. There are glitches for the non-ideal case.
In reality, the propagation is in the nanosecond region, which is not as large as it shown in the figure. It is about 10ns for each type.

**9.3 Procedure to Design Synchronous Counters**

The procedure to design a synchronous counter is listed here.

- Obtain the truth table of the logic sequence for intended counter to be designed. Alternatively obtain the state diagram of the counter.
- Determine the number and type of flip-flop to be used.
- From the excitation table of the flip-flop, determine the next state logic.
- From the output state, use Karnaugh map for simplification to derive the circuit output functions and the flip-flop output functions.
- Draw the logic circuit diagram.
- Simulate the circuit using software.
- Build the circuit.

From the function tables shown in Fig. 7.4, 7.10, 7.17, and 7.20 of the flip-flops learnt earlier in Chapter 7, the excitation or characteristic table of SR flip-flop, D flip-flop, JK flip-flop, and T flip-flop are shown in Fig. 9.7. and 9.8 respectively. \( Q_i \) is denotes the output of the present state and \( Q_{i+1} \) denotes the output of next state.
9.4 Design of Synchronous Counters

In this section, designing of various types of synchronous counter using different types of flip-flop are discussed. Using the procedure and function tables mentioned in section 9.2, a step by step ways to design the synchronous counter discussed.

9.4.1 Design of a Synchronous Decade Counter Using JK Flip-Flop

A synchronous decade counter will count from zero to nine and repeat the sequence. The state diagram of this counter is shown in Fig. 9.9.
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Since there are ten states, four JK flip-flops are required. The truth tables of present and next state for the decade counter are shown in Fig. 9.10. Using the excitation table of JK flip-flop and the outputs of J and K are filled.

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_3$</td>
<td>$Q_2$</td>
<td>$Q_1$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>1</td>
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<td>0</td>
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</tbody>
</table>

**Figure 9.10:** Truth table and state table of a synchronous decade counter

The Karnaugh maps of the output $J_0$, $K_0$, $J_1$, $K_1$, $J_2$, $K_2$, $J_3$, and $K_3$ are shown in Fig. 9.11, 9.12, 9.13, and 9.14 respectively. The simplified results are at the bottom of the Karnaugh maps.

**Figure 9.11:** Karnaugh maps of $J_0$ and $K_0
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Figure 9.12: Karnaugh maps of $J_1$ and $K_1$

Figure 9.13: Karnaugh maps of $J_2$ and $K_2$

Figure 9.14: Karnaugh maps of $J_3$ and $K_3$
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Based on the results obtained from the Karnaugh maps, the circuit design of synchronous decade counter is shown in Fig. 9.15.

![Figure 9.15: A synchronous decade counter designed using JK flip-flop](image)

9.4.2 Design of an Asynchronous Decade Counter Using JK Flip-Flop

An asynchronous decade counter will count from zero to nine and repeat the sequence. Since the JK inputs are fed from the output of previous flip-flop, therefore, the design will not be as complicated as the synchronous version. At the nineth count, the counter is reset to begin counting at zero. The NAND gate is used to reset the counter at the ninth count. At the ninth count the outputs of flip-flop $Q_3$ and $Q_1$ will be high simultaneously. This will cause the output of NAND to go to logic “0” that would reset the flip-flop. The logic design of the counter is shown in Fig. 9.16.

![Figure 9.16: An asynchronous decade counter](image)
9.4.3 Design of a Synchronous Modulus-Six Counter Using SR Flip-Flop

The modulus six counter will count 0, 2, 3, 6, 5, and 1 and repeat the sequence. This modulus six counter requires three SR flip-flops for the design. The truth table of a modulus six counter is shown in Fig. 9.17. From the excitation table of SR flip-flop shown in Fig. 9.8, the logic of output $S_2$, $R_2$, $S_1$, $R_1$, $S_0$, and $R_0$ are filled and shown in Fig. 9.8.

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_2$</td>
<td>$Q_1$</td>
<td>$Q_0$</td>
</tr>
<tr>
<td>0</td>
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<td>0</td>
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<td>1</td>
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</tbody>
</table>

**Figure 9.17:** Truth table and state table of the modulus-six counter

The state diagram is shown in Fig. 9.18.

**Figure 9.18:** State diagram of modulus-six counter
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The Karnaugh maps of the output \( R_0, S_0, R_1, S_1, R_2, \) and \( S_2 \) are shown in Fig. 9.19, 9.20, and 9.21 respectively. The simplified results are at the bottom of the Karnaugh maps.

With the known output logic functions, the logic design of the synchronous modulus six counter is shown in Fig. 9.21.
Figure 9.22: Logic design of synchronous modulus six counters
Tutorials

9.1. State the procedure for design a synchronous counter.

9.2. Draw the timing diagrams of the decade counter shown in Fig. 9.14.

9.3. Design a modulus seven synchronous counter that can count 0, 3, 5, 7, 9, 11, and 12 using D flip-flop.

9.4. Using the truth table shown in Fig. 9.16, design this counter using T flip-flop.

References