Chapter 4

UEEA2223/UEEG4223
Integrated Circuit Design

IC Fabrication,
Layout and
Simulation

UNIVERSITI TUNKU ABDUL RAHMAN
Prepared by
Dr. Lim Soo King
15 Jan 2011.
<table>
<thead>
<tr>
<th>Section</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Chapter 4</strong></td>
</tr>
<tr>
<td><strong>IC Fabrication, Layout, and Simulation</strong></td>
</tr>
<tr>
<td>4.0 Introduction</td>
</tr>
<tr>
<td>4.1 Types of Rules</td>
</tr>
<tr>
<td>4.2 SCMOS Design Rule Sets</td>
</tr>
<tr>
<td>4.2.1 n-well</td>
</tr>
<tr>
<td>4.2.2 n-diff and p-diff</td>
</tr>
<tr>
<td>4.2.3 Polysilicon (Poly 1)</td>
</tr>
<tr>
<td>4.2.4 Polysilicon (Poly 2)</td>
</tr>
<tr>
<td>4.2.5 Option</td>
</tr>
<tr>
<td>4.2.6 Contact</td>
</tr>
<tr>
<td>4.2.7 Metal1</td>
</tr>
<tr>
<td>4.2.8 Via1</td>
</tr>
<tr>
<td>4.2.9 Metal2</td>
</tr>
<tr>
<td>4.2.10 Via2</td>
</tr>
<tr>
<td>4.2.11 Metal3</td>
</tr>
<tr>
<td>4.2.12 Via3</td>
</tr>
<tr>
<td>4.2.13 Metal4</td>
</tr>
<tr>
<td>4.2.14 Via4</td>
</tr>
<tr>
<td>4.2.15 Metal5</td>
</tr>
<tr>
<td>4.2.16 Via5</td>
</tr>
<tr>
<td>4.2.17 Metal6</td>
</tr>
<tr>
<td>4.2.18 Pad</td>
</tr>
<tr>
<td>4.3 CMOS Circuit Layout</td>
</tr>
<tr>
<td>4.4 Layout Concepts and Methods</td>
</tr>
<tr>
<td>4.5 Using Schematic Capture and Layout Software</td>
</tr>
<tr>
<td>4.5.1 Schematic Capture</td>
</tr>
<tr>
<td>4.5.2 Layout</td>
</tr>
<tr>
<td>4.5.3 Drawing Layout of Logic Gates and Combinational Circuit</td>
</tr>
<tr>
<td>4.6 Parasitic Components of MOS Transistor</td>
</tr>
<tr>
<td>4.6.1 Parasitic Resistance</td>
</tr>
<tr>
<td>4.6.2 Parasitic Capacitance</td>
</tr>
<tr>
<td>4.6.3 Junction Leakage Current</td>
</tr>
<tr>
<td>4.7 Voltage Decay on an RC Ladder</td>
</tr>
<tr>
<td>4.8 RC Model of Metal Interconnect and Poly Line</td>
</tr>
<tr>
<td>4.9 Electromigration and Latch-up</td>
</tr>
<tr>
<td>4.10 Scaling Theory</td>
</tr>
<tr>
<td>Exercises</td>
</tr>
<tr>
<td>Bibliography</td>
</tr>
<tr>
<td>Figure 4.1:</td>
</tr>
<tr>
<td>Figure 4.2:</td>
</tr>
<tr>
<td>Figure 4.3:</td>
</tr>
<tr>
<td>Figure 4.4:</td>
</tr>
<tr>
<td>Figure 4.5:</td>
</tr>
<tr>
<td>Figure 4.6:</td>
</tr>
<tr>
<td>Figure 4.7:</td>
</tr>
<tr>
<td>Figure 4.8:</td>
</tr>
<tr>
<td>Figure 4.9:</td>
</tr>
<tr>
<td>Figure 4.10:</td>
</tr>
<tr>
<td>Figure 4.11:</td>
</tr>
<tr>
<td>Figure 4.12:</td>
</tr>
<tr>
<td>Figure 4.13:</td>
</tr>
<tr>
<td>Figure 4.14:</td>
</tr>
<tr>
<td>Figure 4.15:</td>
</tr>
<tr>
<td>Figure 4.16:</td>
</tr>
<tr>
<td>Figure 4.17:</td>
</tr>
<tr>
<td>Figure 4.18:</td>
</tr>
<tr>
<td>Figure 4.19:</td>
</tr>
<tr>
<td>Figure 4.20:</td>
</tr>
<tr>
<td>Figure 4.21:</td>
</tr>
<tr>
<td>Figure 4.22:</td>
</tr>
<tr>
<td>Figure 4.23:</td>
</tr>
<tr>
<td>Figure 4.24:</td>
</tr>
<tr>
<td>Figure 4.25:</td>
</tr>
<tr>
<td>Figure 4.26:</td>
</tr>
<tr>
<td>Figure 4.27:</td>
</tr>
<tr>
<td>Figure 4.28:</td>
</tr>
<tr>
<td>Figure 4.29:</td>
</tr>
<tr>
<td>Figure 4.30:</td>
</tr>
<tr>
<td>Figure 4.31:</td>
</tr>
<tr>
<td>Figure 4.32:</td>
</tr>
<tr>
<td>Figure 4.33:</td>
</tr>
<tr>
<td>Figure 4.34:</td>
</tr>
<tr>
<td>Figure 4.35:</td>
</tr>
<tr>
<td>Figure 4.36:</td>
</tr>
<tr>
<td>Figure 4.37:</td>
</tr>
<tr>
<td>Figure 4.38:</td>
</tr>
<tr>
<td>Figure 4.39:</td>
</tr>
<tr>
<td>Figure 4.40:</td>
</tr>
<tr>
<td>Figure 4.41:</td>
</tr>
<tr>
<td>Figure 4.42:</td>
</tr>
<tr>
<td>Figure 4.43:</td>
</tr>
<tr>
<td>Figure 4.44:</td>
</tr>
<tr>
<td>Figure 4.45:</td>
</tr>
<tr>
<td>Figure 4.46:</td>
</tr>
</tbody>
</table>
Figure 4.47: The linear time invariant model of a MOS transistor.......................... 125
Figure 4.48: (a) Drain/source structure of MOS transistor (b) bottom structure and (c) side-wall structure.............................................................. 126
Figure 4.49: Drain of the MOS transistor under reverse biased condition................ 129
Figure 4.50: An n-MOS transistor switching model ........................................... 130
Figure 4.51: ac RC model of two series connected n-MOS transistors..................... 131
Figure 4.52: (a) Lump element model and (b) Tree model of metal interconnect ......... 132
Figure 4.53: The phenomenon of electromigration and its effects.......................... 133
Figure 4.54: Illustration of parasitic components of CMOS device (a) device geometry and (b) latch-up model............................................................... 134
Figure 4.55: Refilled deep trench between p-well and n-well.................................. 134
Figure 4.56: Generalized scaling theory for MOS transistor ................................. 136
Chapter 4

IC Fabrication, Layout, and Simulation

4.0 Introduction

In this Chapter, we will discuss the design rules that are a set of specifications that govern the layout of integrated circuit masking layout. It is the minimum separation or thickness governing the components distance and width requirements. This chapter presents a set of scalable CMOS design rules and the guides for layout of the design.

The CMOS layout technique with the emphasis using stick diagram and the concept of vertical layout approach are discussed. In the same section, the electronic design automation EDA tools – Microwind - is introduced with specification design examples.

MOS transistor device RC model is introduced in the last section that including the derivation of diffusion capacitance and resistance. The RC models of metal interconnect and polysilicon gate are also including. The issues of electromigration, CMOS latch-up, and scaling theory are the last to be discussed.

4.1 Types of Rules

Integrated circuit layout deals with the design of geometrical objects on each masking layer according to a set of rules. Geometrical object is referred to as polygon that created by one or more rectangles as what is shown in Fig. 4.1.

![Figure 4.1: Examples of geometrical object – polygon](image)

The design rules can be classified into four major types. They are:
4 IC Fabrication, Layout, and Simulation

- Minimum Feature – This is the smallest side length of an object on the layer. If the object is a line, then this specifies the minimum line width.
- Minimum Spacing – The minimum spacing rule governing how close two polygons can be placed.
- Surround – A surround rule is used when a feature on one layer must be embedded within a polygon on another layer.
- Exact Size – An exact size rule means that the feature can only have the dimensions specified in the rule. Other sizes are not permitted.

Violation of the design rules of minimum feature specified in the above section may lead broken or damage line. Placing two polygons too close to each other may lead to incomplete resolved feature leading to unwanted electrical capacitance coupling between two features. In the long run operation of the device that has design rule violation feature leads to functionality problem and reliability issue.

Let’s take the example illustrated in Fig. 4.2 to check the minimum feature and minimum spacing rules. Of all the thickness specified in the example shown in Fig. 4.2, thickness $d$ and $e$ do not meet the minimum thickness requirements as specified by $W$. This is a design rule violation.

![Figure 4.2: Example to illustrate minimum feature and spacing]

Of all the spacing A, B, and C, spacing C does not meet the minimum as specified as $S$. This is a design rule violation. In all layout software for integrated circuit design, design rule check routine is readily available.

The surround rule is illustrated by an oxide contact cut for access to $p$-diffusion as illustrated in Fig. 4.3.
Figure 4.3: Surround rule example

The surrounding spacing S shown is the minimum spacing required for the contact cut embedded on the \( p \)-diffusion layer. This is necessary to allow some mask misalignments so that it is still fall within the boundary of the existing layer in this case is the \( p \)-diffusion layer.

The exact size rule is usually applied to contact cut and vias. In this example, the minimum size is D.

In the present time, there are three design rule sets, which are generic scalable CMOS SCMOS, submicron rule and deep submicron. Generic SCMOS is applicable to line width more than 1.0\( \mu \)m. Submicron is typically used for about 0.8\( \mu \)m to 0.35\( \mu \)m. Deep submicron rule is used for less than 0.35\( \mu \)m.

In the SCMOS rules used here, all spacings are integer multiples of \( \lambda \) and called lambda design rules. We shall study the rule set for a dual-poly, 6-metal, \( n \)-well CMOS processes.

### 4.2 SCMOS Design Rule Sets

The typical set of design rule listed in this section is the generic SCMOS set, which applicable to CMOS process of line width more than 1.0\( \mu \)m. Since the standard Microwind process is set at 0.12\( \mu \)m technology, which is belong to deep submicron technology. Student is encouraged to find out the design rule set for this technology. The format of each design rule is listed as rule# Description: Value. The value listed here is the minimum value.
4 IC Fabrication, Layout, and Simulation

4.2.1 n-well

The n-well design rules are
- r101 Minimum well size: $12\lambda$
- r102 Well-to-well spacing: $11\lambda$
- r103 Minimum surface area: $144\lambda^2$

The illustration is shown in Fig. 4.4.

![Figure 4.4: Illustration of n-well design rules](image)

4.2.2 n-diff and p-diff

n-diff and p-diff design rules are
- r201 Minimum $n^+$ and $p^+$ diffusion width: $4\lambda$
- r202 Minimum spacing between two $p^+$ and $n^+$ diffusion: $4\lambda$
- r203 Extension over n-well after $p^+$ diffusion: $6\lambda$
- r204 Minimum spacing between $n^+$ diffusion and n-well: $6\lambda$
- r205 Border of well after $n^+$ bias: $2\lambda$
- r206 Minimum spacing between $p^+$ diffusion and n-well: $6\lambda$
- r210 Minimum surface: $24\lambda^2$

The illustration is shown in Fig. 4.5.
4 IC Fabrication, Layout, and Simulation

4.2.3 Polysilicon (Poly 1)

Polysilicon (Poly 1) design rules are
- r301 Polysilicon width: 2λ
- r302 Polysilicon gate on diffusion: 2λ
- r303 Polysilicon gate on diffusion for high voltage FET: 4λ
- r304 Between two poly boxes: 3λ
- r305 Polysilicon versus other diffusion: 2λ
- r306 Diffusion after polysilicon: 4λ
- r307 Extra gate after diffusion: 2λ

The illustration is shown in Fig. 4.6.
4 IC Fabrication, Layout, and Simulation

4.2.4 Polysilicon (Poly 2)

Polysilicon (Poly 2) design rules are
- r311 Polysilicon width: $2\lambda$
- r312 Polysilicon gate extended beyond diffusion: $2\lambda$

The illustration is shown in Fig. 4.7.

Figure 4.7: Illustration of polysilicon (Poly 2) design rule

4.2.5 Option

Option design rules are
- ropt: $2\lambda$
  Border of “option” layer over diff $n^+$ and diff $p^+$.

The illustration is shown in Fig. 4.8.

Figure 4.8: Illustration of option design rule

4.2.6 Contact

Contact design rules are
- r401 Contact size: $2\lambda \times 2\lambda$
- r402 Spacing between two contact: $3\lambda$
4 IC Fabrication, Layout, and Simulation

- r403 Contact to diffusion edge: $2\lambda$
- r404 Poly surround: $2\lambda$
- r405 Metal1 surround: $2\lambda$
- r406 Contact to poly gate: $3\lambda$

The illustration is shown in Fig. 4.9.

![Figure 4.9: Illustration of Contact design rule](image)

4.2.7 Metal1

Metal1 design rules are

- r501 Metal1 width: $3\lambda$
- r502 Between two metal1: $4\lambda$
- r510 Minimum surface: $32\lambda^2$

The illustration is shown in Fig. 4.10.

![Figure 4.10: Illustration of Metal1 design rule](image)

4.2.8 Via1

Via1 design rules are

- r601 Via1 size: $2\lambda \times 2\lambda$
- r602 Spacing between Via1 edge: $4\lambda$
- r603 Between Via1 and contact: $0\lambda$

- 103 -
4 IC Fabrication, Layout, and Simulation

- r605 Extra Metal2 over Via1: $2\lambda$

The illustration is shown in Fig. 4.11.

4.2.9 Metal2

Metal2 design rules are
- r701 Metal2 width: $3\lambda$
- r702 Between two metal2: $4\lambda$
- r710 Minimum surface: $32\lambda^2$

The illustration is shown in Fig. 4.12.

4.2.10 Via2

Via2 design rules are
- r801 Via1 size: $2\lambda \times 2\lambda$
- r802 Spacing between Via2 edge: $4\lambda$
- r804 Extra Metal2 over Via2: $2\lambda$
- r805 Extra Metal3 over Via2: $2\lambda$

The illustration is shown in Fig. 4.13.
4.2.11 Metal3

Metal3 design rules are
- r701 Metal3 width: 3\(\lambda\)
- r702 Between two metal3: 4\(\lambda\)
- r710 Minimum surface: 32\(\lambda^2\)

The illustration is shown in Fig. 4.14.

![Illustration of Metal3 design rule](image)

**Figure 4.14:** Illustration of Metal3 design rule

4.2.12 Via3

Via3 design rules are
- ra01 Via3 size: 2\(\lambda\) x 2\(\lambda\)
- ra02 Spacing between Via3 edge: 4\(\lambda\)
- ra04 Extra Metal3 over Via3: 2\(\lambda\)
- ra05 Extra Metal4 over Via3: 2\(\lambda\)

The illustration is shown in Fig. 4.15.

![Illustration of Via3 design rule](image)

**Figure 4.15:** Illustration of Via3 design rule

4.2.13 Metal4

Metal4 design rules are
- rb01 Metal4 width: 3\(\lambda\)
- rb02 Between two metal4: 4\(\lambda\)
- rb10 Minimum surface: 32\(\lambda^2\)

The illustration is shown in Fig. 4.16.
4.2.14 Via4

Via4 design rules are
- rc01 Via4 size: \(2\lambda \times 2\lambda\)
- rc02 Spacing between Via4 edge: \(4\lambda\)
- rc04 Extra Metal4 over Via4: \(2\lambda\)
- rc05 Extra Metal5 over Via4: \(2\lambda\)

The illustration is shown in Fig. 4.17.

4.2.15 Metal5

Metal5 design rules are
- rd01 Metal5 width: \(8\lambda\)
- rd02 Between two metal5: \(8\lambda\)
- rd10 Minimum surface: \(100\lambda^2\)

The illustration is shown in Fig. 4.18.
### 4.2.16 Via5

Via5 design rules are
- re01 Via5 size: $5\lambda \times 5\lambda$
- re02 Spacing between Via5 edge: $5\lambda$
- re04 Extra Metal5 over Via5: $2\lambda$
- re05 Extra Metal6 over Via5: $2\lambda$

The illustration is shown in Fig. 4.19.

![Figure 4.19: Illustration of Via5 design rule](image)

### 4.2.17 Metal6

Metal6 design rules are
- rf01 Metal6 width: $8\lambda$
- rf02 Between two metal6: $15\lambda$
- rf10 Minimum surface: $300\lambda^2$

The illustration is shown in Fig. 4.20.

![Figure 4.20: Illustration of Metal6 design rule](image)

### 4.2.18 Pad

Pad design rules are
- rp01 Pad size: $100\mu m \times 100\mu m$
- rp02 Spacing between Pads: $100\mu m$
- rp03 Surround (passivation): $5\mu m$
- rp04 Spacing between Pad and Active: $20\mu m$
4 IC Fabrication, Layout, and Simulation

The illustration is shown in Fig. 4.21.

![Diagram of Pad design rule](image)

Figure 4.21: Illustration of Pad design rule

One does not require memorizing all this design rules. As you practice more, you will naturally get use with the design rules. Moreover, any violation of the rule can be checked by a click of button of the software.

4.3 CMOS Circuit Layout

In designing the layout of the CMOS circuit, horizontal or vertical approach can be adopted. Power lines such as $V_{DD}$ and $V_{SS}$ can be placed in horizontal manner. The components of the circuit are to be placed within the space between the power lines. The poly gate line is placed vertically. The metal1 line is placed horizontally. The metal2 line shall then be placed vertically. The placing of metal line will be alternative horizontal and vertical approach to avoid delay.

One can always begin by sketching the layout so that when drawing the actual layout, the design rules are watched. One has to realize that drawing the layout is actually a form of art. You may start the design with the smallest dimension such as the poly, and then followed by the diffusion region and contact. In this manner, you can cross check the design rule at any time and adjust accordingly.

4.4 Layout Concepts and Methods

Upon designing the transistor level circuit, the next step is to make physical layout of the circuit so that it can be converted into mask for final fabrication of the circuit. The starting point of the layout is circuit schematic. The circuit shows that connection between transistors. One approach is making used of the stick diagram as illustrated in Fig. 4.22 for the layout of an inverter.
One observation is that the $V_{DD}$ and $V_{SS}$ power lines are placed one on top and one at the bottom. The input is placed at the left side of the circuit, whilst the output is placed at the right side.

Stick diagram symbols for wire are shown in Fig. 4.23. The figure has shown up to metal3. It can be extended to metal6 or metal7. One may use color to draw the stick diagram. Usually red is used for poly, green for $n$-diffusion, yellow for $p$-diffusion and shaded blue for metal. Illustrated in Fig. 4.24 is the stick diagram for an NAND gate. One may also arrange the stick diagram such that the poly formed the vertical line with input at the bottom of the circuit as illustrated in Fig. 4.25 for the same NAND gate layout.
Drawing a large circuit using stick diagram usually would lead to spaghetti layout. Thus, it is necessary to make use of hierarchical approach to organize the stick diagram.

Drawing the complex logic circuit using stick diagram is equally complex like the drawing a large circuit mentioned earlier. It is necessary to seek a common path which termed as *Euler path* for simplifying the final stick diagram to obtain optimization. Optimization means less propagation delay and more efficient way of utilizing the silicon area in terms of having single piece of...
diffusion. Euler path is a path through all nodes in the graphical design such that each edge is passed once and only once. Using the logic function $A \cdot (D+E) + (B \cdot C)$ as an illustration, the most efficient path, the Euler path is $EDABC$, which is shown in Fig. 4.26. An example of the path which is not efficient is $ADEBC$.

Let’s consider to draw the layout of series-parallel or parallel-series transistor level circuit. The parallel-series $p$-MOS transistor network circuit is shown in Fig. 4.27. The logic function of this circuit is Output $= \overline{(A + B) \cdot C}$. 

**Figure 4.26:** The Euler path of logic function $A \cdot (D+E) + (B \cdot C)$
The layout of this network circuit is shown in Fig. 4.28. To do the layout, first thing to is to identify the source and drain of the transistors and label them as shown in Fig. 4.27. There are two parallel transistors A and B connected to a series transistor C. One of the arrangements of layout is drain-source of transistor A connected to source-drain of transistor B and then connected to source-drain of transistor C. Source of transistor A and B shall then be connected to $V_{DD}$ via metal 1, whilst the drains of transistor A and B, and source of transistor C are connected together via metal 1. Drain of transistor C shall be connected to output via metal 1. In this manner one may be see there is minimum usage of metal. This shall mean the contribution of resistance and capacitance of the metal to the delay time is at minimum.
4 IC Fabrication, Layout, and Simulation

Figure 4.28: The layout of circuit shown in Fig. 4.27

4.5 Using Schematic Capture and Layout Software

There are countless of VLSI layout software available in the market. The price to obtain this software ranges from free of charge to millions of dollar. Learner can browse this website http://www.vlsitechnology.org/html/ic_software.html for obtaining the information. For learning purpose, we shall choose Microwind software. Light version of Microwind software, which is free of charge, can be obtained from website http://www.microwind.org. This software package comes with two parts, which the schematic capture software and layout software. The schematic software – “Dsch.exe” allows user to design logic circuit, which can be combinational and sequential types using basic logic gates or $p$- and $n$-MOS transistors. The layout software - “Microwind.exe” allows user to design layout manually or draw layout automatically by importing a verilog file.

4.5.1 Schematic Capture

The manual page of the schematic capture software “Dsch.exe” is shown in Fig. 4.29. The manual contains functions, open file, save file, select, cut, copy, move, rotate, add line, simulate, timing diagram, zoom in, zoom out, view electrical list, move, symbol libraries, and working area. The symbol libraries
consist of basic gate and input pad and output display. The symbol libraries also consist of some advanced electrical components and sources. At the right bottom of the display shows the default technology used. In this screen it shows the default technology is 0.12µm.

You can begin to design logic gate using $p$-MOS and $n$-MOS transistors. If we are to design a CMOS inverter as shown in Fig. 4.30, which has logic function $output = \overline{A}$, the logic function can be interpreted as a low asserted high and high asserted low equation. This shall mean a $p$-MOS and an $n$-MOS transistor are connected in series with input $A$ and output taken from the drains of the transistors. The source of $p$-MOS transistor is connected to $V_{DD}$ power line, whilst the source of $n$-MOS transistor is connected to $V_{SS}$ ground line. To get the transistor, it is done by pressing the transistor and placing it into the working area. To interconnect, it is done by ‘add line’ function. The power $V_{DD}$ and $V_{SS}$ ground can be connected in the similar manner i.e. pressing them from the symbol libraries and placing them at the right place in the working area.
Upon design, you can press the ‘simulate’ key to simulate the functionality of the inverter. The result of the simulation can be viewed by pressing the ‘timing diagram’ button, which is shown in Fig. 4.31. From the timing diagram, it shows that the inverter is functioning correctly.

The logic function of a three input NAND is output = $\overline{A \cdot B \cdot C}$. This equation is a high asserted low equation, which can be used to design $n$-MOS transistor network of the NAND gate. For designing the CMOS version of this NAND gate, we need also a $p$-MOS network circuit, which is a low asserted high network equation. This can be done by using DeMorgan theorem to convert logic function output = $\overline{A \cdot B \cdot C}$ to output = $\overline{A} + \overline{B} + \overline{C}$, which is a low asserted high equation. The transistor level of a three input NAND gate is shown in Fig. 4.32. It is done by dragging the $n$-MOS and $p$-MOS transistors to the working
area and inter-connected them and putting the $V_{DD}$ power line and $V_{SS}$ ground line.

![Image of a 3-input NAND gate](image)

**Figure 4.32:** The design of a 3-input NAND gate

The result of simulation is shown from the timing diagram in Fig. 4.33. From the timing diagram, it shows that the 3-input NAND gate is functionally working.

![Timing diagram of the 3-input NAND gate](image)

**Figure 4.33:** Timing diagram of the 3-input NAND gate

### 4.5.2 Layout

The manual page of the layout “Microwind.exe” is shown in Fig. 4.34. The manual contains the functions, open file, save file, select, cut, copy, move and
stretch, simulate, timing diagram, zoom in, zoom out, view electrical node, 2D view, 3D view, ruler, design rule check, palette function, and the working area. The palette consists of basic $n^+$ and $p^+$ diffusion layers, polysilicon 1 and 2 layers, metal 1 to metal 6 layers, power sources, via connections, passive and active components, and MOS transistor generator. At the right bottom of the display shows the default technology used. In this screen it shows the default technology is 0.12µm.

![Image of Microwind layout software](image)

**Figure 4.34:** The manual page of Microwind layout software

In the vertical approach layout, poly gate line is placed vertically, while power line is placed horizontally. This approach will be adopted for the rest of design mentioned in this text.

Let’s proceed to design the layout of an inverter as shown in Fig. 4.30. One of approaches is to use the ‘MOS generator’ function in the palette. Upon selecting ‘MOS generator’ function, you can choose either $n$-MOS transistor, $p$-MOS transistor, or double gate transistor. Since the inverter has one input, you will choose one finger type. Beside these options, you may choose low leakage, high speed or high voltage type. The layout is shown in Fig. 4.35. From the colour illustration you will see that the $p$-MOS transistor is sitting inside an $n$-well. The ‘cross square’ pad is the via that connecting the semiconductor either the $p$-diffusion or $n$-diffusion type to the first metal 1, which is in blue color. The orange color bar is the polysilicon gate. The grid is used for ease for drawing layout and there is a scale of 5 lambda, which equivalent to 0.30µm from a grid point to another grid point. You may choose ‘zoom in’ or ‘zoom
out’ function to change the scale. Since the substrate material for CMOS VLSI design is a (100) $p$-type semiconductor, thus, the black work area is a (100) $p$-type substrate.

Upon designing or placing the transistors, the next step is to inter-connect them according to the design and placing the power line horizontally, bias the $p$-substrate and $n$-well, connect input source, and connect visible node for visible observation. Figure 4.26 shows the layout after these layout steps. The layout shows that the source of the $p$-MOS transistor is connected to power source $V_{DD}$ via metal 1, whilst the source of $n$-MOS transistor is connected to $V_{SS}$ ground source via metal 1. The drains of both the transistors are connected together to form the output. The $p$-substrate is biased with $V_{SS}$ source, whilst the $n$-well is biased with $V_{DD}$ source. You may want recall the reason why the $p$-substrate and $n$-well needed to be biased in this manner.

Figure 4.25: Layout of a $p$-MOS transistor and an $n$-MOS transistor
Upon design the layout of the inverter, you may want simulate to see if the layout is functioning. This can be done by selecting simulation function button. The result of the simulation is shown in Fig. 4.37, which is right as expected for an inverter.

Let’s discuss how to design the layout of three series connected transistor as shown in Fig. 4.38. You may begin with the ‘MOS generator’ function and follow by choosing \( n \)-MOS transistor with three fingers. You shall then remove
4 IC Fabrication, Layout, and Simulation

the extra via contact and metal 1 using ‘cut’ function. Figure 4.39 shows the layout after connected the source of transistor C to $V_{SS}$ ground, bias the $p$-substrate with $V_{SS}$ ground, and placing the input source to input A, B, and C.

Figure 4.38: The transistor circuit of three series $n$-MOS transistors

Figure 4.39: The layout of three series $n$-MOS transistors

Let’s discuss how to design the layout of three parallel connected transistors as shown in Fig. 4.40. You may begin with the ‘MOS generator’ function and
follow by choosing $p$-MOS transistor with three fingers. Figure 4.41 shows the layout after connecting the $V_{DD}$ power line, bias the n-well with $V_{DD}$ voltage, and connecting all sources and drains of the transistors together via metal1.

Figure 4.40: The transistor circuit of three parallel connected $p$-MOS transistors

Figure 4.41: The layout of three parallel connected $p$-MOS transistors

4.5.3 Drawing Layout of Logic Gates and Combinational Circuit

Based on the knowledge of layout learnt from previous Section 4.5.2, following the same procedure, the layout of any logic gates and combinational circuit can be drawn. Taking for an example the transistor level circuit of the combinational logic with logic function output = $A \cdot (B+C)$ is designed and shown in Fig. 4.42. Its layout is shown in Fig. 4.43. The simulation result is shown in Fig. 4.44.
4 IC Fabrication, Layout, and Simulation

Figure 4.42: The transistor level design of combinational circuit output = $A \cdot (B + C)$

Figure 4.43: The layout of combinational circuit output = $A \cdot (B + C)$
4.6 Parasitic Components of MOS Transistor

MOS transistor is normally used for switching and voltage gain. There are number of parasitic components associated with the structure. It contains parasitic resistance and capacitance that affects the circuit operation. These components cannot be eliminated especially in high-speed device operation. We shall discuss these two components in detail.

4.6.1 Parasitic Resistance

The resistance of MOS transistor is not linear as we can see from the output characteristic of the MOS transistor, despite the fact, the term linear time-invariant LTI is used to provide information about the drain to source flow. Since the resistance is not linear, therefore, the resistance R_n is depending on the point where it is taken. Using n-MOS transistor as an example, the non linear resistance is governed by

\[ R_n = \frac{dV_{DS}}{dI_{DS}} \]

which is the reciprocal of conductance shown in equation (2.35). i.e. \( R_n = \frac{L}{\mu_n C_{ox} W(V_{GS} - V_{t_n})} \). The saturation resistance \( R_n \) is obtained from equation

\[ R_n = \frac{2L V_{DS}}{\mu_n C_{ox} W(V_{GS} - V_{t_n})^2} \]

Since the digital electronics works in linear region, therefore, the linear equation is used for calculating the drain to source resistance \( R_n \) or \( R_{ds} \). Since the logic voltage is either \( V_{DD} \) or \( V_{SS} \), the \( V_{GS} \) voltage or \( V_{SG} \) voltage is equal to \( V_{DD} \). Thus, turn-on resistance \( R_n \) is equal to

**Figure 4.44:** The timing diagram of combinational circuit output = A \cdot (B + C)
4 IC Fabrication, Layout, and Simulation

\[ R_n = \frac{L}{\mu_e C_{ox} W (V_{DD} - V_{th})} \]  
\[ (4.1) \]

and

\[ R_p = \frac{L}{\mu_p C_{ox} W (V_{DD} - |V_{tp}|)} \]  
\[ (4.2) \]

4.6.2 Parasitic Capacitance

MOSFET has a number of parasitic capacitances. They are shown in Fig. 4.45. These capacitances are function of voltage and dimensions. \( C_{DB} \) and \( C_{SB} \) are depletion capacitances due to \( pn \) junction of the MOS transistor. The other three capacitance \( C_{GS} \), \( C_{GD} \), and \( C_{GB} \) are related to MOS capacitance \( C_{OX} = \frac{\varepsilon_{ox} WL}{d_{ox}} \).

![Figure 4.45: Capacitance of MOS transistor](image)

In VLSI or semiconductor physics, MOS capacitance is usually expressed in farad per unit area. By default \( C_{OX} \) is equal to \( \frac{\varepsilon_{ox}}{d_{ox}} \). The gate to backward capacitance \( C_{GB} \) is equal to \( C_{OX} WL \). \( C_{GB} \) is also equal to gate capacitance \( C_G \) at cut-off region when gate-to-source voltage is equal to zero.

Figure 4.46 illustrates the relationship of gate-channel capacitance with respect to various gate-to-source voltage.
Based on the results, it shows that the capacitance $C_{GS}$ and $C_{GD}$ are approximately equal to $\frac{2}{3}C_g$ at saturation region. For triode region, the capacitance $C_{GS}$ and $C_{GD}$ are approximately equal to $\frac{1}{2}C_g$ and $\frac{1}{2}C_g$ respectively at zero bias, which is $\frac{1}{2}C_{ox}$. Please note the capacitance mentioned in this paragraph has unit of farad.

Based on capacitance distribution of a MOS transistor shown in Fig. 4.45, the linear time-invariant model of the $n$-MOS transistor shall be as shown in Fig. 4.47.
Source and drain capacitance \( C_S \) and \( C_D \) are respectively equal to \( C_S = C_{GS} + C_{SB} \) and \( C_D = C_{GD} + C_{DB} \). These capacitance values are used partially to determine the switching times of the MOS transistor device.

In linear operation, which is the operation for digital device, \( C_{GS} \) and \( C_{GD} \) are equal to half of \( C_G \), which is \( \frac{1}{2} \cdot C_{ox} \cdot WL \) as illustrated in Fig. 4.46. The depletion capacitance \( C_{SB} \) and \( C_{DB} \) are respectively equal to the sum of bottom capacitance and sidewall capacitance of the drain or source of the device. They are calculated by approach discussed in the following paragraph.

The drain or source structure of the MOS transistor is shown in Fig. 4.48(a). You can view the drain and source as a rectangular tray with a bottom plate of side \( W \) by \( X \) and side wall of \( W \) by \( x_j \) and \( X \) by \( x_j \). Its corresponding bottom structure and side-wall structure are shown in Fig. 4.48(b) and Fig. 4.48(c) respectively.

The capacitance \( C_n \) of the source or drain of the \( n \)-MOS transistor is equal to the sum of bottom capacitance \( C_{bot} \) and the side wall capacitance \( C_{sw} \).
The bottom capacitance $C_{bot}$ is equal to $C_j X W$, where $C_j$ is the junction capacitance per unit area, $X$ is the length of the drain or source. $C_n$ is also equal to $C_{DB}$ or $C_{SB}$ values.

The side wall capacitance $C_{sw}$ of $W$ side is equal to

$$C_{swL} = C_{jsw} W$$

where $C_{jsw}$ is junction capacitance per unit area multiplied by the thickness $x_j$ of drain or source i.e. $C_{jsw} = C_j x_j$. The total side wall is $(2W+2X)$. Therefore, the total side wall capacitance is $C_{sw} = C_{jsw}(2W+2X) = C_{jsw} P$, where $P$ is the perimeter of the drain or source. The total capacitance of the drain or source $C_n$ is

$$C_n = C_{jbot} X W + C_{jsw}(2W+2X)$$

The capacitance shown in equation (4.5) is the zero voltage bias capacitance. This is the value usually used to model the timing of the MOS transistor since zero voltage bias has the maximum capacitance.

Junction capacitance at time is called *depletion capacitance*. The junction capacitance $C_j$ of the $n$-type source or drain with the $p$-type substrate is based on equation $C_j = \left(\frac{q\varepsilon_s N_A}{2(V_{bi} + V_R)}\right)^{1/2}$. If we denote $C_o$ as the zero bias voltage junction capacitance, which is $\left(\frac{q\varepsilon_s N_A}{2V_{bi}}\right)^{1/2}$, then junction capacitance $C_j$ becomes

$$C_j = \left[\frac{q\varepsilon_s N_A}{2(V_{bi} + V_R)}\right]^{1/2} = \frac{C_o}{\sqrt{1 + \frac{V_R}{V_{bi}}}}$$

where $V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$ and $V_R$ denotes as built-in potential and bias voltage respectively. In general equation (4.6) can be written as
4 IC Fabrication, Layout, and Simulation

\[ C_j = \frac{C_{om}}{m} \left( 1 + \frac{V_n}{V_{bi}} \right)^m \]  

(4.7)

where \( m \) denotes grading parameter which is a value less than one. For \( m = 1/2 \), it denotes an abrupt or step junction, whilst for \( m = 1/3 \), it denotes a gradual junction. \( C_{om} \) denotes the junction capacitance at zero bias voltage for an \( m \) graded junction.

Usually, we take the side-wall junction of the drain/source of the MOS transistor as a linearly graded junction, whilst the bottom junction of the drain/source of the MOS transistor has an abrupt junction. Thus, their grading parameter \( m \) are 1/3 and 1/2 respectively. Combining equation (4.5) and equation (4.7), the drain/source capacitance of the MOS transistor follows equation (4.8).

\[ C_n(V_R) = \frac{C_{jbot}WX}{\left( 1 + \frac{V_R}{V_{bibo}} \right)^{1/2}} + \frac{C_{jsw}2(W + X)}{\left( 1 + \frac{V_R}{V_{bisw}} \right)^{1/3}} \]  

(4.8)

Since the output changes from \( V_1 \) to \( V_2 \) and vice versa, the average drain/source capacitance \( C_{navg} \) is equal to

\[ C_{navg}(V_R) = \frac{1}{(V_2 - V_1)} \left\{ \int_{v_1}^{v_2} C_{jbot}WX \cdot dV_R + \int_{v_1}^{v_2} C_{jsw}2(W + X) \cdot dV_R \right\} \]  

(4.9)

Let \( K_{1/2}(V_1, V_2)C_{jbot}WX = \frac{1}{(V_2 - V_1)} \int_{v_1}^{v_2} C_{jbot}WX \cdot dV_R \) and \( K_{1/3}(V_1, V_2)C_{jsw} \cdot 2(W + X) = \frac{1}{(V_2 - V_1)} \int_{v_1}^{v_2} 2C_{jsw}(W + X) \cdot dV_R \). Equation (4.9) shall become

\[ C_{navg}(V_R) = K_{1/2}(V_1, V_2)C_{jbot}WX + K_{1/3}(V_1, V_2)C_{jsw} \cdot 2(W + X). \]

For \( m \) grading parameter,
\[ K_m(V_1, V_2) = \frac{1}{V_2 - V_1} \int_{V_1}^{V_2} \frac{1}{1 + \frac{V_R}{V_{bds}}} m \cdot dV_R \quad (4.10) \]

The integration result of equation (4.10) yields equation (4.11).

\[ K_m(V_1, V_2) = \frac{V_{bi}}{(-m+1)(V_2 - V_1)} \left[ \left( 1 + \frac{V_2}{V_{bi}} \right)^{(-m+1)} - \left( 1 + \frac{V_1}{V_{bi}} \right)^{(-m+1)} \right] \quad (4.11) \]

where \( K_m(V_1, V_2) \) is called linear time-invariant factor LTI. Usually the bias voltage \( V_2 \) and \( V_1 \) are respectively equal to \( V_{OH} \) and \( V_{OL} \). Therefore, equation (4.11) is equal to

\[ K_m(V_{OL}, V_{OH}) = \frac{V_{bi}}{(-m+1)(V_{OH} - V_{OL})} \left[ \left( 1 + \frac{V_{OH}}{V_{bi}} \right)^{(-m+1)} - \left( 1 + \frac{V_{OL}}{V_{bi}} \right)^{(-m+1)} \right] \quad (4.12) \]

### 4.6.3 Junction Leakage Current

The \textit{pn} junctions formed by the drain to bulk and source to bulk interfaces in a MOS transistor introduce leakage current that is often important in high-performance circuit design. Consider the drain of a MOS transistor shown in Fig. 4.49 is reverse biased by drain-to-source voltage.

\[ I_R \]

\[ \text{Drain} \]

\[ \text{Substrate} \]

\[ V_{DS} \]

\[ + \]

\[ - \]

\[ d_{dep} \]

\[ n^+ \]

\[ p \]

\[ I_R \]

**Figure 4.49**: Drain of the MOS transistor under reverse biased condition

The junction leakage current \( I_R \) is equal to
4 IC Fabrication, Layout, and Simulation

\[ I_R = I_o + I_{\text{gen}} \]  \hspace{1cm} (4.13)

where \( I_o \) is the reverse saturation current and \( I_{\text{gen}} \) is the re-generation current. The re-generation current is equal to

\[ I_{\text{gen}} \approx \frac{qA_n d_{\text{depMin}}}{2\tau} \left[ \frac{1 + \frac{V_{DS}}{V_{bi}}}{1} - 1 \right] \]  \hspace{1cm} (4.14)

Usually the reverse saturation current is very small that can be ignored. The reverse bias current of the drain-to-substrate junction is equal to

\[ I_R \approx \frac{qA_n d_{\text{depMin}}}{2\tau} \left( \left[ \frac{V_{DS}}{V_{bi}} \right]^m - 1 \right) \]  \hspace{1cm} (4.15)

where \( m \) is grading factor.

The switching model of the MOS transistor taken into account the parasitic capacitance, resistance, and leakage current shall be as shown in Fig. 4.50.

![An n-MOS transistor switching model](image)

**Figure 4.50:** An n-MOS transistor switching model

### 4.7 Voltage Decay on an RC Ladder

The ac RC ladder circuit for two \( n \)-channel MOS transistors connected in series is shown in Fig. 4.51. \( R_1 \) and \( R_2 \) represent the channel resistance of MOS transistor \( Mn_1 \) and MOS transistor \( Mn_2 \) respectively. \( C_1 \) and \( C_2 \) represent the source capacitance of MOS transistor \( Mn_1 \) and MOS transistor \( Mn_2 \) respectively. An input voltage \( V_{in} \) is fed to the drain of transistor \( Mn_1 \). After some time the voltage \( V_1 \) and \( V_2 \) shall be same as \( V_{in} \). If the input voltage \( V_{in} \) is removed and node D is shorted to ground, the charged stored in capacitance \( C_1 \)
and $C_2$ would begin to discharge through resistance $R_1$ and $(R_1 + R_2)$ respectively.

Figure 4.51: ac RC model of two series connected $n$-MOS transistors

Since $V_2$ is the output voltage, it can be shown that $V_2$ is discharged following equation $V_2(t) = V_{in}e^{-t/\tau}$, where the time constant $\tau$ is equal to $\tau = C_1R_1 + C_2(R_1 + R_2)$. The time constant $\tau$ is derived from Elmore formula for series RC chain. The analysis can be done by applying Kirchhoff’s current law at node $V_1$ and $V_2$, to obtain equation as function $C_1$, $C_2$, $R_1$, and $R_2$, which are

$$-C_1 \frac{dV_1}{dt} = \frac{V_1 - V_2 - V_1}{R_1}$$

and

$$-C_2 \frac{dV_2}{dt} = \frac{V_2 - V_1}{R_2}.$$ 

One way to obtain the solution for the equations is by means of Laplace transforming from time domain to $s$-domain, which will take the form

$$-sC_1V_1(s) + C_1V_1(0) = \frac{V_1 - V_2 - V_1}{R_1}$$

and

$$-sC_2V_2(s) + C_2V_2(0) = \frac{V_2 - V_1}{R_2}.$$ 

where $V_1(0)$ and $V_2(0)$ are initial condition of the time domain and these values are $V_{in}$ value. In general the time constant for $N$ series connected MOS transistor would follow the general Elmore formula which takes the form.

$$\tau = \sum_{k=1}^{N} C_k \left( \sum_{m=1}^{k} R_m \right)$$

(4.16)

If it is charging then the output voltage $V_N$ for an $N$ connected series MOS transistors is

$$V_N(t) = V_{in} \left( 1 - e^{-t/\tau} \right)$$

(4.17)

For an example, the time constant $\tau$ for four series connected MOS transistors with resistance $R_1$, $R_2$, $R_3$, and $R_4$ and capacitance $C_1$, $C_2$, $C_3$, and $C_4$ is equal to

$$\tau = R_1C_1 + C_2(R_1 + R_2) + C_3(R_1 + R_2 + R_3) + C_4(R_1 + R_2 + R_3 + R_4).$$
4.8 RC Model of Metal Interconnect and Poly Line

A metal line with length L, width W and thickness d has resistance $R_{metal}$ equal to $R_{metal} = \rho \frac{L}{Wd}$, where $\rho/d$ is defined as the sheet resistance $R_{smetal}$. Thus, the resistance of the metal interconnect line of length L and width W is equal to

$$R_{metal} = R_{smetal} \frac{L}{W}$$

(4.18)

The capacitance of the metal interconnect of length L width W, and thickness of oxide $X_{int}$ separating the metal line and substrate is equal to

$$C_{metal} = \frac{\varepsilon_{ox}}{X_{int}} LW$$

(4.19)

Equation (4.19) can be re-written as $\frac{\varepsilon_{ox}}{X_{int}}$, which is the capacitance per unit area.

Based on the above analysis, two RC models of the metal line interconnect connecting point A and point B is shown in Fig. 4.51. The lump RC model is treating the capacitance as a lump sum putting at the end of point B. However, this approach would end with double the time delay. A better approach is using tree model or $\pi$-model, whereby the capacitance is treated as distributed capacitance whereby the capacitance $C_{metal}$ is distributed half at point A and half at point B. With this approach, the time delay is a half of the lump sum model approach.

![Figure 4.52: (a) Lump element model and (b) Tree model of metal interconnect](image-url)
The extraction of capacitance of poly line follows the same approach of extraction of diffusion capacitance for the drain/source of the MOS transistor. There are two components, which are plate component and side wall perimeter component due fringe electrical field caused by thickness of the poly line which is usually larger than its width in the modern VLSI design.

**4.9 Electromigration and Latch-up**

The metal interconnect must be able to carry high current density which is approximately $10^5 \text{A/cm}^2$ because high speed requires high current density. High current density leads to a phenomenon called *electromigration*, which is a major cause of breakdown of integrated circuit. Figure 4.53 illustrates the phenomenon and its effects.

![Figure 4.53: The phenomenon of electromigration and its effects](image)

Electromigration forces metal ions to move downstream mainly along the grain structure. When this happens, it develops voids and hillocks at the curves and forks. Electromigration can be prevented by controlling grain structure along the micro-crystalline that forms metal lines. Larger atom such as copper has large grain meaning less surface area and therefore less resistance to electromigration. Copper also locks the aluminum atoms in place and prevents non-uniform thermal effect. It prevents hillocking.

Not to forget that there is another problem, which is latch-up. Latch-up is seen as a sudden massive increase in the current draw of an integrated circuit that is high enough to rupture metal interconnect line and even bond wire due high current density. Latch-up is a destructive problem. Although latch-up problem has been well understood but this problem exists due to parasitic component particularly the resistance as the results of scaled down. Figure 4.54 illustrates the parasitic components that lead to latch-up problem.
4 IC Fabrication, Layout, and Simulation

**Figure 4.54:** Illustration of parasitic components of CMOS device (a) device geometry and (b) latch-up model

If the product $R_{\text{sub}}$ and $I_S$ are larger than the base-to-emitter voltage of the horizontal transistor, then this transistor would turn-on. As the result, the collector of this transistor is closed to ground voltage. This may provide the switching path for vertical transistor if the product of $R_{\text{well}}$ and $I_W$ current is greater than the emitter-to-base voltage of this transistor. If this process is happening, the 5V $V_{\text{DD}}$ is almost shorted to ground voltage via the very low resistance of collector-to-emitter terminals of the both transistors. As the result, high current density is registered that can rupture the metallization and bond wire.

A method employed to overcome the latch-up problem is the formation of deep-trench that is deeper than the well or tub as shown in Fig. 4.55. This technique can eliminate latch-up because the $n$-channel and $p$-channel devices are physically isolated by the filled trench.

**Figure 4.55:** Refilled deep trench between $p$-well and $n$-well
4.10 Scaling Theory

In order to achieve higher density logic integration, the approach is to develop sub-micron size device structures. Effects which are negligible in large MOS transistor become distinct and extremely important when the transistor dimensions are reduced. Scaling theory provides a general guide to make MOS transistor smaller. It is not possible or desirable to follow every aspect of the theory. However, it remains a useful metric for measuring progress in device physics especially the simulation or prediction of the behavior of the device with smaller dimension.

Scaling theory deals with the question of how the device characteristics are changed as the dimensions of the device are reduced in an idealized well-defined manner. Scaling theory is ideal ignoring many small-device effects that govern the performance of MOS transistor. It is often desirable to adhere to the large device models for simplicity but modify the parameters to account for the more important changes in the transistor parameters. Scaling of the device to smaller dimension affects parameters such as threshold voltage and mobility. Smaller channel length decreases the threshold voltage. Narrower device increases threshold voltage. Small channel length increases horizontal electric field that causes the MOS transistor to operate with saturation velocity. This reduces the drain current of the device. High electric field means high energetic carrier that can enter the oxide to become trapped charge and affects the threshold voltage of the MOS transistor.

The drain and source of the MOS transistor are usually much heavily doped than the bulk. Couple with high electric field, hot ion tunneling is unavoidable. This issue causes leakage. In order to resolve this problem, lightly doped drain LDD approach is adopted for the design of small dimension MOS transistor.

Several schemes can be constructed from scaling rules shown in Fig. 4.56. S is the dimensional scaling factor and k is factor by which voltages are scaled. One of the earlier scaling methodologies is based on constant-field scaling, which keep electrical field constant. In this method S is made equal to k. This approach is theoretical viable that has to increase the speed, reduction of voltage swing and capacitance. It is being used to scale to 1.0µm. Scaling to 1.0µm is in fact closed to constant-voltage scaling, which is by making k = 1. In this approach voltage swing stays the same, but device current increases due to increase of oxide capacitance $C_{ox}$. Since drive current increases roughly as the
square of supply voltage, constant-voltage produces more speed improvement than constant-field scaling.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Variables</th>
<th>Scaling Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimensions</td>
<td>W, L, d_{ox}, x_j</td>
<td>1/S</td>
</tr>
<tr>
<td>Potentials</td>
<td>V_{ds}, V_{gs}</td>
<td>1/k</td>
</tr>
<tr>
<td>Doping concentration</td>
<td>N_A, N_D</td>
<td>S^2/k</td>
</tr>
<tr>
<td>Electric field</td>
<td>E</td>
<td>S/k</td>
</tr>
<tr>
<td>Current</td>
<td>I_{ds}</td>
<td>S/k^2</td>
</tr>
<tr>
<td>Gate delay</td>
<td>t_{delay}</td>
<td>k/S^2</td>
</tr>
</tbody>
</table>

**Figure 4.56:** Generalized scaling theory for MOS transistor

Using constant-voltage approach and considering a MOS transistor with a channel width W and a channel length L such that the channel area is A = LW and introducing the concept of a scaling factor S > 1, a new scaled device is created with reduced dimensions W' and L' where W' = \( \frac{W}{S} \) and L' = \( \frac{L}{S} \). The reduced scaled area A' is equal to A' = \( \frac{A}{S^2} \). Similarly, the oxide thickness is d'_{ox} = \( \frac{d_{ox}}{S} \). Thus, the reduced oxide capacitance is C'_{ox} = S \cdot \frac{C_{ox}}{d_{ox}} = SC_{ox}. Similarly, the reduced process parameter K' = SK and device parameter is \( \beta' = S\beta \). Threshold voltage V_{t} and drain-to-source voltage V_{DS} are to be scaled. With all parameters being scaled down, the scaled down drain current is I'_{D} = \( \frac{I_D}{S} \).

**Exercises**

4.1. Extract the design rules of the 6 metals 0.12µm technology from Microwind layout software.

4.2. Taking into consideration of the SCMOS design rule, determine the aspect ratio of an n-MOS transistor device.

4.3. Taking into consideration of the SCMOS design rule, determine the aspect ratio of a p-MOS transistor device.

4.4. Given a two input NOR gate, using stick diagram to draw the layout of its CMOS circuit.
4.5. Given a logic function \( f(A, B, C) = (A \cdot B) + \overline{C} \). Using Euler path to optimize the final stick diagram of the circuit.

4.6. Determine the Euler path for logic function \( f(A, B, C, D, E) = (A + B \cdot C + D \cdot E) \).

4.7. Design the transistor level circuit of combinational circuit that has function output = \( A + (C + D) \cdot B \).

4.8. Design the layout of a 2-input AND gate.

4.9. Consider an \( n \)-MOS transistor that has a channel width \( W = 8 \mu m \), a channel length of \( L = 0.5 \mu m \) and is made with a process where \( K_n = 180 \times 10^{-6} A/V^2 \), \( V_{tn} = 0.70V \) and \( V_{DD} = 3.3V \). Calculate the channel resistance.

4.10. Calculate the output capacitance of the inverter shown in the figure. All dimensions are shown in micron and the load capacitance is 50fF.

4.11. Given that the sheet resistance of the polysilicon is \( 4.0 \Omega/\square \) and the capacitance per unit area of the polysilicon is \( 0.1 \text{fF/\mu m}^2 \). Calculate the time constant of a polysilicon polygon with structure shown in the figure, width equals to \( 3 \lambda \) and the corner resistance is taken as 0.65 square.
Bibliography