### Chapter 5 Digital CMOS IC Design

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5.0 Introduction

In the CMOS design, \( p \)-MOS and \( n \)-MOS transistor are used complimentary. \( P \)-MOS transistor is a logic 0 asserted high output device, which means that when \( p \)-MOS transistor is switched on with logic 0. According to the biasing condition of \( p \)-MOS transistor, the source voltage \( V_S \) should be larger than drain voltage \( V_D \). Thus, the source of \( p \)-MOS transistor is usually connected to \( V_{DD} \) power rail. Therefore, when the \( p \)-MOS transistor is switched on, the output will provide logic 1.

\( n \)-MOS transistor is a logic 1 asserted low output device. This shall mean that logic 1 is used to switch on \( n \)-MOS transistor. According to the biasing condition of \( n \)-MOS transistor, drain voltage \( V_D \) should be larger than source voltage \( V_S \). This shall mean logic 1 asserted low output transistor should be connected to ground rail or \( V_{SS} \) rail. Thus, when the \( n \)-MOS transistor is switched on, the output will provide logic 0.

In this chapter, we shall discuss the transistor level design of logic circuit and static combinational circuit. The chapter will cover the tri-state circuit. The designs using pseudo \( n \)-MOS transistor, pass-transistor and transmission gate are discussed in details. Other method for designing the logic circuit such as mirror logic circuit is discussed.

5.1 The Design Hierarchy

Integrated circuit can be complex like the microprocessor chip. Complete understanding of every aspect of the chip design and fabrication requires several years of study and practical experience. Designing an integrated circuit, which is general termed as chip, for a specific function, this chip is considered as a system. Hierarchical design approach is usually adopted in designing VLSI integrated circuit. This approach is also known as divide-and-conquer approach. This approach is commonly used in programming, whereby a procedure is written not as a huge list of primitive statement but as calls to simpler procedure. Each procedure breaks down the task into smaller operations
until each step is refined into a procedure simple enough to be written directly. Based on this concept, the structure of the design hierarchy is shown in Fig. 5.1.

![Design Hierarchy Diagram]

**Figure 5.1:** Structure of the design hierarchy

Each level in the structure concentrates in specific design issue. System level concentrates on the main operation or function of the chip. This level, the functional blocks of the system are drawn. The input/output characteristic is decided. Specifications of the system are written down. Specifications are used
to create an abstract high level model. The abstract model contains information on the behavior of each block and the interaction among the block in the system.

Logic level is the level where logic network circuit of each functional block is designed. At the end of design, a net list is generated that describes the logic gates and wire needed to implement the design.

Circuit design level is the step where logic network is transformed into transistor as the switching devices. Digital variables are represented by voltage levels that change with time.

Once the circuit design is completed, it is transformed into a design file for silicon integrated circuit physical design level. Physical design level involves transforming the electronic circuit into on-screen colored geometrical patterns using computer graphics and analysis tools. This step is also called the layout step.

The final step of the chip design is chip fabrication where physical integrated circuit is fabricated and put into package for eventual wiring into product used for application.

The approach is the top-down design approach. This is the appropriate way for complex design such as microprocessor. Take for an example; the 64-bit processor cannot be designed bit by bit from the bottom-up approach. Small device is possible to be designed in this manner. However, for learning purpose, bottom-up design approach works well.

Hierarchical design approach helps the designer to organize the function of a large number of transistors into particular, easy-to-summary function. The approach makes it easy to re-use pieces of chip, either by modifying an old design or to be used as a component for a new design.

### 5.2 Transistor Level Design of Logic Gate

The Boolean function of the NOT gate is $f(x) = \overline{x}$. According to Shannon’s expansion theorem, the Boolean function $f(X)$ is $f(X) = X \cdot 0 + \overline{X} \cdot 1$. From the equation, one can see that there is logic 1 asserted low output and logic 0 asserted high output. Therefore, the design can be implemented with an $n$-MOS transistor for logic 1 asserted low output and a $p$-MOS transistor for logic 0 asserted high output. The CMOS circuit diagram of the NOT gate is shown in Fig. 5.2 and its corresponding layout is shown in Fig. 5.3.
The Shannon’s expansion for a NOR gate is 

\[ f(A, B) = \overline{A} \cdot \overline{B} \cdot 1 + \overline{A} \cdot B \cdot 0 + A \cdot \overline{B} \cdot 0 + A \cdot B \cdot 0 = (\overline{A} \cdot \overline{B} \cdot 1) + (A \cdot 0 + B \cdot 0). \]

Based on the criteria mentioned in earlier for the design of NOT gate, NOR gate can be designed with p-MOS transistors connected in series, which would be logic 0 asserted to get ANDed output logic 1 and two-n-MOS transistors connected in parallel, which would be logic 1 asserted to get Ored output logic 0. The CMOS circuit of a NOR gate is shown in Fig. 5.4 and its corresponding layout is shown in Fig. 5.5.
The Shannon’s expansion for a OR gate is $f(A, B) = \overline{A} \cdot \overline{B} \cdot 0 + \overline{A} \cdot B \cdot 1 + A \cdot \overline{B} \cdot 1 + A \cdot B \cdot 1 = (A \cdot \overline{B} \cdot 0) + (A \cdot 1 + B \cdot 1)$. Based on the series, the design required logic 0 asserted low output and logic 1 asserted high output. This shall mean that to implement the function, beside the requirement of two $n$-MOS and two $p$-MOS transistors, it also requires two additional NOT gates. Thus, the total number of MOSFET transistor required is increased to eight, which are four $n$-MOS and
four $p$-MOS transistors. The logic circuit of eight-transistor OR gate is shown in Fig. 5.6.

![Figure 5.6: 8-MOS transistor design of an OR gate](image)

The Boolean function for OR gate can be written as $f(A, B) = \overline{A + B}$, which shall mean that the function can be implemented with a NOR gate connected to a NOT gate. With this design, the number of MOS transistor required is six instead of eight mentioned earlier, which is shown in Fig. 5.7.

![Figure 5.7: CMOS circuit of an OR gate](image)
The Shannon’s expansion for a NAND gate is \( f(A, B) = \overline{A} \cdot \overline{B} \cdot 1 + \overline{A} \cdot B \cdot 1 + A \cdot \overline{B} \cdot 1 + A \cdot B \cdot 0 = (\overline{A} \cdot \overline{B} + 1) + (A \cdot B \cdot 0) \). Based on the procedure mentioned in earlier section for the design of NOR gate, the NAND gate can be designed with \( p \)-MOS transistors connected in parallel, which would be logic 0 asserted to get ORed output logic 1 and two-\( n \)-MOS transistors connected in series, which would be logic 1 asserted to get ANDed output logic 0. The CMOS circuit of a NAND gate is shown in Fig. 5.8 and its corresponding layout is shown in Fig. 5.9.

![CMOS circuit of a NAND gate](image)

**Figure 5.8:** CMOS circuit of a NAND gate

![Layout of a 2-input NAND gate](image)

**Figure 5.9:** The layout of a 2-input NAND gate
The Shannon’s expansion for a AND gate is $f(A, B) = \overline{A} \cdot \overline{B} \cdot 0 + \overline{A} \cdot B \cdot 0 + A \cdot \overline{B} \cdot 0 + A \cdot B \cdot 1 = \overline{A} \cdot 0 + \overline{B} \cdot 0 + \overline{A} \overline{B} \cdot 1$. Following the same argument as the case of how to design the OR gate, in order to save the number of MOSFET used for the design and to reduce the propagation delay of the gate, the AND gate should be designed using a NAND gate connected to a NOT gate. The CMOS circuit of the AND gate is shown in Fig. 5.10.

![CMOS circuit of an AND gate](image)

**Figure 5.10:** CMOS circuit of an AND gate

### 5.3 Transistor Level Design of CMOS Complex Logic Circuit

One of the most powerful aspects of building logic circuit in CMOS is the ability to create a single circuit that provides several logic operations in the integrated manner. This is called complex or combinational logic gates. Let’s consider the Boolean function $f(A, B, C) = \overline{A} \cdot (B + C)$. Based on this function, one can see that the simplest way to design the function is one OR gate and one NAND gate. This shall mean that to design this function, a total of ten MOS transistors are required. Owing to the design constraint on a VLSI design, one ought to consider the performance and the number of MOS transistor on the silicon chip. Thus, the traditional approach should not be used as the straight
forward design. The AND-OR-NOT AOI and OR-AND-NOT OAI circuit approaches shall be used, which required utilizing the Shannon’s expansion of the Boolean function to determine the OAI circuits.

According to Shannon’s expansion theorem, the Boolean function \( f(A, B, C) = \overline{A} \cdot \overline{(B+C)} \) can be expressed as
\[
f(A, B, C) = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot 1 + \overline{A} \cdot B \cdot \overline{C} \cdot 1 + A \cdot B \cdot \overline{C} \cdot 1 + A \cdot B \cdot C \cdot 0 + A \cdot B \cdot \overline{C} \cdot 0 + A \cdot B \cdot C \cdot 0 = [\overline{A} + (B \cdot \overline{C})] \cdot 1 + A \cdot (B+C) \cdot 0.
\]
From the equation, the first five terms are used to make an AOI circuit and the last three terms are used to make for an OAI circuit. Alternatively, the AOI circuit can be determined by the complement of OAI circuit. From Shannon’s expansion circuit, the AOI function is
\[
\overline{A} \cdot B \cdot \overline{C} \cdot 0 + A \cdot B \cdot \overline{C} \cdot 0 = A \cdot (B+C) \cdot 0.
\]
The complement of function \( A \cdot (B+C) \cdot 0 \), which is \( A \cdot (B+C) \cdot 1 \) is equal to \([\overline{A} + (B \cdot \overline{C})] \cdot 1 \) after applying DeMorgan’s theorem. The Boolean function \( f(A, B, C) = \overline{A} \cdot (B+C) \) can now be designed using six MOS transistors. The circuit of the design is shown in Fig. 5.11.

![CMOS circuit of Boolean function](image)

**Figure 5.11:** CMOS circuit of Boolean function \( f(A, B, C) = \overline{A} \cdot (B+C) \)
The layout of the function \( f(A, B, C) = A \cdot (B + C) \) is shown in Fig. 5.12.

\[ f(A, B, C) = A \cdot (B + C) \]

The Boolean function of an exclusive OR gate is \( f(A, B) = A \oplus B \). The function can be re-written as \( f(A, B) = \overline{A} \oplus \overline{B} = \overline{A} \cdot \overline{B} + A \cdot B \). Thus, the AOI for the n-MOS transistor network is \( \overline{A} \cdot \overline{B} + A \cdot B \). Using pushing bubble technique, the p-MOS transistor OAI network is equal to \( (A + B) \cdot (\overline{A} + \overline{B}) \).

One would notice that the total number of MOS transistor required is twelve for the exclusive OR gate design shown in Fig. 5.13. However, the total number of MOS transistor can be reduced to a lesser number if pass-transistor, mirror logic circuit, pseudo n-MOS logic or transmission gates design approach are adopted.
The Boolean function of a full adder is \( S = A \oplus B \oplus C_i \) and \( C_o = (B \cdot C_i) + (A \cdot B) + (A \cdot C_i) = (A+B) \cdot C_i + A \cdot B \), where \( S \) is the sum, \( C_o \) is the carry-out, and \( C_i \) is the carry-in. The sum \( S \) is also equal to \( S = (\overline{A} \cdot \overline{B} \cdot C_i) + (\overline{A} \cdot B \cdot \overline{C_i}) + (A \cdot \overline{B} \cdot C_i) + (A \cdot B \cdot C_i) \), which can be expressed in terms of carry out \( C_o \) equal to \( S = (A + B + C_i) \cdot \overline{C_o} + A \cdot B \cdot C_i \).

In order to save the number of MOS transistor used in the design, one of the methods is using pseudo n-MOS transistor circuit, which has carry-out \( C_o \) circuit shown in Fig. 5.14. There is a total reduction of five p-MOS transistors. Student should attempt to design this CMOS version of the circuit. The designer has to take note the p-MOS transistor used in the pseudo n-MOS transistor design has to be sufficiently large enough to handle the current flow into the n-MOS transistor network and at the same time has sufficient worst case resistance for providing logic 0. Using circuit shown in Fig. 5.14, the worst case current drain in the n-MOS transistor network is the drain current of five n-MOS transistors simultaneously switched-on. Alternatively, the designer can design the circuit with four parallel standard p-MOS transistors.
The similar approach can be used to design the sum part of the full adder. The pseudo $n$-MOS transistor version of the circuit is shown in Fig. 5.15. We shall discuss the physics of pseudo $n$-MOS transistor design in details in Section 5.5.
5.4 Pass-Transistor

In this section, the characteristics of MOS transistor when the transistor is used as pass-transistor are analyzed. The study covers the transfer of voltage from source to drain and vice versa with the gate used as the control, and the application of pass-transistor for designing logic circuit.

5.4.1 \( n \)-channel MOS Pass-Transistor

Let’s analyze the \( n \)-channel MOS pass-transistor shown in Figure 5.16. The input has a voltage and the output is connected to a capacitive load that has a voltage across it. The capacitor represents the total capacitance at the output node and has several contributions. Placing a logic 1 at the gate switches on the \( n \)-channel MOS transistor into conduction, connecting the input and output nodes.

![Figure 5.16: n-channel MOS transistor pass-transistor](image)

5.4.1.1 Pass Logic 1

Let’s analyze the circuit when a logic 1 is passed through this transistor. The gate-to-source voltage \( V_{GS} \) is equal to \( V_{GS} = V_{DD} - V_{out}(t) \), whilst the drain-to-source voltage is \( V_{DS} = V_{DD} - V_{out}(t) \). Once can see that the transistor is in saturation mode. Thus, the drain-to-source current \( I_{DS} \) is

\[
I_{DS} = C_{out} \frac{dV_{out}}{dt} = \frac{B_n}{2} \left( V_{DD} - V_{out}(t) - V_{in} \right)^2 \quad (5.1)
\]

Integrating equation (5.1) with the condition at time \( t = 0 \) output voltage \( V_{out}(t) = 0V \), the output voltage \( V_{out}(t) \) is found to be equal to...
\[ V_{\text{out}}(t) = (V_{\text{DD}} - V_{\text{in}}) \frac{t/(2\tau_n)}{1 + t/(2\tau_n)} \]  

(5.2)

\( \tau_n \) is the time constant which is equal to \( C_{\text{out}}R_n = \frac{C_{\text{out}}}{\beta_n (V_{\text{DD}} - V_{\text{in}})} \). From equation (5.2), it can be shown that the maximum output voltage \( V_{\text{out(max)}}(t) \) is equal to \( (V_{\text{DD}} - V_{\text{in}}) \) for time \( t \rightarrow \infty \). Since the maximum output voltage for an \( n \)-channel MOS pass-transistor is \( V_{\text{DD}} - V_{\text{in}} \), therefore, it is usually claimed that this type of pass-transistor passes a weak logic 1 and the loss of the output is said to be \textit{threshold voltage loss}. It is obvious to maintain conduction, the gate-source voltage \( V_{\text{GS}} \) must have a minimum value of \( V_{\text{in}} \).

5.4.1.2 Pass Logic 0

Let’s analyze the circuit when logic 0 is passed through this transistor. The gate-to-source voltage \( V_{\text{GS}} \) is equal to \( V_{\text{GS}} = V_{\text{DD}} \), whilst the drain-to-source voltage is \( V_{\text{DS}} = V_{\text{out}}(t) \). Once can see that the transistor is in linear mode since \( V_{\text{DS}} \) is equal to \( V_{\text{sat}} \), which is \( V_{\text{out(max)}} \) at time \( t = 0 \). The drain-to-source current \( I_{\text{DS}} \) shall be

\[ I_{\text{DS}} = -C_{\text{out}} \frac{dV_{\text{out}}(t)}{dt} = \beta_n \left( (V_{\text{GS}} - V_{\text{in}})V_{\text{out}}(t) - \frac{V_{\text{out}}^2(t)}{2} \right) \]  

(5.3)

Integrating this equation with the applied condition yields the output voltage \( V_{\text{out}}(t) \) equal to

\[ V_{\text{out}}(t) = (V_{\text{DD}} - V_{\text{in}}) \frac{2\exp(-t/\tau_n)}{1 + \exp(-t/\tau_n)} \]  

(5.4)

\( \tau_n \) is the time constant, which is equal to \( C_{\text{out}}R_n = \frac{C_{\text{out}}}{\beta_n (V_{\text{DD}} - V_{\text{in}})} \). For time \( t \rightarrow \infty \), \( V_{\text{out}}(t) = 0V \). Thus, it is claimed that \( n \)-channel MOS pass-transistor can pass a strong logic 0.

5.4.1.3 Switching Time

This section analyzes the low-to-high transition time \( t_{\text{LH}} \) and the high-to-low transition time \( t_{\text{HL}} \) of the \( n \)-channel MOS pass-transistor. Equation (5.2) is used to calculate the low-to-high transition time \( t_{\text{LH}} \). Rearrange equation (5.2) yields,
To find $t_{LH}$ time, it is done by setting $V_{out}(t) = 0.9V_{out(max)}$. Thus, the low-to-high transition time $t_{LH}$ is equal to $t_{LH} = 18\tau_n$.

The high-to-low transition time $t_{HL}$ is determined by setting $V_{out}(t) = 0.1V_{out(max)}$ using equation (5.4). Rearranging equation (5.4), it yields,

$$t = \tau_n \ln \left[ \frac{2V_{out(max)}}{V_{out}(t)} - 1 \right]$$  \hspace{1cm} (5.6)

After substituting $V_{out}(t) = 0.1V_{out(max)}$, the high-to-low transition time $t_{HL}$ is equal to $t_{HL} = \tau_n \ln(19) = 2.94\tau_n$.

The result shows that it takes 6.1 times duration to pass logic 1 than logic 0 through an $n$-channel MOS pass-transistor.

### 5.4.2 $p$-channel MOS Pass-Transistor

Let’s analyze the $p$-channel MOS pass-transistor shown in Figure 5.17. The input has a voltage and the output is connected to a capacitive load that has a voltage across it. The capacitor represents the total capacitance at the output node and has several contributions. Placing logic 0 at the gate switches on the $p$-channel MOS transistor into conduction, connecting the input and output nodes.

**Figure 5.17: $p$-channel MOS transistor pass-transistor**
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5.4.2.1 Pass Logic 1

Let’s analyze the circuit when logic 1 is passed through this transistor. The source-to-gate voltage is equal to $V_{SG} = V_{DD}$, whilst the source-to-drain voltage is $V_{SD} = V_{DD} - V_{out(t)}$. If assume at time $t = 0$, $V_{out(t)} = |V_{tp}|$. Once can see that at time $t = 0$, the transistor is either linear mode or in saturation mode. But one is very sure that as time increases, the transistor is in linear mode. Thus, the drain-to-source current $I_{DS}$ is

$$ I_{DS} = C_{out} \frac{dV_{out}}{dt} = \frac{\beta_p}{2} \left(2(V_{DD} - |V_{tp}|)(V_{DD} - V_{out(t)}) - (V_{DD} - V_{out(t)})^2\right) $$

(5.7)

Integrating equation (5.7) with the condition at time $t = 0$, output voltage is $V_{out(t)} = |V_{tp}|$, the output voltage $V_{out(t)}$ is found to be equal to

$$ V_{out(t)} = V_{DD} - (V_{DD} - |V_{tp}|) \frac{2\exp(-t/\tau_p)}{1 + \exp(-t/\tau_p)} $$

(5.8)

$\tau_p$ is the time constant, which is equal to $C_{out}R_p = \frac{C_{out}}{\beta_p(V_{DD} - |V_{tp}|)}$. From equation (5.8), it can be shown that the maximum output voltage $V_{out(max)}(t)$ is equal to $V_{DD}$ for time $t \to \infty$. Since the maximum output voltage $V_{out(max)}$ for a $p$-channel MOS pass-transistor is $V_{DD}$, therefore, it is usually claimed that $p$-channel pass-transistor can pass a strong logic 1.

5.4.2.2 Pass Logic 0

Let’s analyze the circuit when logic 0 is passed through this transistor. This is done by assuming that $V_{out(t)} = V_{DD}$ at time $t = 0$. The source-to-gate voltage $V_{SG}$ is equal to $V_{SG} = V_{out(t)}$, whilst the source-to-drain voltage is $V_{SD} = V_{out(t)}$. It is obvious to see that the transistor is in saturation mode, which is $V_{out(max)}$ at time $t = 0$. The drain-to-source current $I_{DS}$ shall be

$$ I_{DS} = - C_{out} \frac{dV_{out(t)}}{dt} = \frac{\beta_p}{2} (V_{SG} - |V_{tp}|)^2 $$

(5.9)

Integrating this equation with the applied condition yields the output voltage $V_{out(t)}$ equal to
For time $t \to \infty$, $V_{\text{out}}(t) = |V_{\text{tp}}|$. Thus, it is claimed that $p$-channel MOS pass-transistor can pass a weak logic 0. This is understood that $p$-channel MOS transistor requires at least a $V_{SG}$ voltage of $|V_{\text{tp}}|$ to maintain conduction.

### 5.4.2.3 Switching Time

This section analyzes the The low-to-high transition time $t_{LH}$ is determined by setting $V_{\text{out}}(t) = 0.9V_{\text{out(max)}}$ using equation (5.8). Rearranging equation (5.8) yields.

$$t = \tau_p \ln \left[ \frac{V_{DD} - 2|V_{\text{tp}}| + V_{\text{out}}(t)}{V_{DD} - V_{\text{out}}(t)} \right]$$

(5.11)

After substituting $V_{\text{out}}(t) = 0.9V_{\text{out(max)}}$, the high-to-low transition time $t_{LH}$ is equal to $t_{LH} = \tau_p \ln(19) = 2.94\tau_p$.

The high-to-low transition time $t_{HL}$ and the high-to-low transition time $t_{HL}$ of the $p$-channel MOS pass-transistor. Equation (5.10) is used to calculate the high-to-low transition time $t_{HL}$. Rearrange equation (5.10) yields.

$$t = 2\tau_p \left[ \frac{V_{DD} - |V_{\text{tp}}|}{V_{\text{out}}(t) - |V_{\text{tp}}|} - 1 \right]$$

(5.12)

To find the $t_{HL}$ time, it is done by setting $V_{\text{out}}(t) = 0.1V_{\text{out(max)}}$. Thus, the high-to-low transition time $t_{HL}$ is equal to $t_{HL} = 18\tau_p$.

The result shows that it takes 6.1 times the duration to pass logic 0 than logic 1 through a $p$-channel MOS pass-transistor.

Owing to threshold voltage loss, it causes static power consumption for in both $p$-MOS pass-transistor and $n$-MOS pass-transistor.

### 5.4.3 Series Connected Pass-Transistor

A series-connection of three $n$-channel pass-transistors is shown in Fig. 5.18. Since the $n$-channel pass-transistor passes strong logic 0, therefore, the output
V_{out} shall be at logic 0 after passing through transistors MnA, MnB, and MnC for V_{in} equal to logic 0.

![Series-connected n-channel pass-transistor](image)

**Figure 5.18:** A series-connected n-channel pass-transistor

For the case of input is logic 1, the maximum output V_A is equal to (V_{DD} – V_{in}). Since the gate is connected to V_{DD}, the maximum output V_B and V_C is also equal to (V_{DD} – V_{in}). Thus, for a series-connected n-channel pass-transistor with input V_{in} equal to logic 1, the maximum output is equal to (V_{DD} – V_{in}).

For series-connected p-channel MOS pass-transistor, the minimum output is equal to |V_{tp}| when the input V_{in} is logic 0.

For a series-connected n-channel MOS pass-transistor configuration shown in Fig. 5.19, the circuit suffers dual threshold-loss when the input is at logic 1.

![Dual threshold-loss n-channel pass-transistor](image)

**Figure 5.19:** Dual threshold-loss n-channel pass-transistor
The maximum output $V_{out}$ is equal to $(V_{DD}-2V_{tn})$, since the maximum gate voltage applied to transistor MnB is $(V_{DD}-V_{tn})$.

For a series-connected $p$-channel MOS pass-transistor with the configuration shown in Fig. 5.18, the minimum output is equal to $2|V_{tp}|$ when the input $V_{in}$ is logic 0.

Thus, student is remained that design with such configuration is not recommended due to double threshold loss.

### 5.4.4 Application of Pass-Transistor

In this section, we shall study the use of pass-transistor for designing the logic circuit. Consider a 2-input exclusive NOR with function is $f(A, B) = A \oplus B$ that can written as $\overline{A} \cdot B + A \cdot \overline{B}$. The function can be designed by Oring two $n$-channel pass-transistors with an ANDing functions $\overline{A} \cdot \overline{B}$ and $A \cdot B$ respectively. The design of function is shown in Fig. 5.20.

![Diagram of exclusive NOR gate design using n-channel pass-transistor](image)

**Figure 5.20:** Exclusive NOR gate design using $n$-channel pass-transistor
The design using n-MOS pass-transistor shown in Fig. 5.20 can only pass strong logic 0 and weak logic 1. One may add two inverters in front of the pass transistor to get the strong logic 0 and logic 1.

For the circuit to be able to pass both strong logic 0 and logic 1, a design with both p-MOS and n-MOS pass-transistors are required. Figure 5.21 shows the design. Again one may add two inverters in front of the pass transistor to get the strong logic 0 and logic 1.

Let’s consider to design a 2-input AND gate. The logic function of the gate is \( f(A, B) = A \cdot B \). The design is shown in Fig. 5.22 using both n-channel and p-channel transistors for obtaining strong logic 0 and logic 1. It is necessary to the p-channel transistor to provide logic 0, which is \( B \cdot \overline{B} = 0 \), otherwise when input B has logic 0, the output will be at high impedance or undefined state.
The design of a 3-input AND gate with function \( f(A, B, C) = A \cdot B \cdot C \) is shown in Fig. 5.23. Note \( p \)-channel MOS transistors are used to pass logic 0, when either input B or C or both are at logic 0. Otherwise, the output will be at high impedance state or undefined state.
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5.5 Pseudo n-MOS Logic Gate

A complex logic circuit required equal number of n-MOS transistor and p-MOS transistor. This post a problem because of large area depicts less density design. Thus, it is at time necessary to keep the fast n-MOS transistor network and replaces the slow p-MOS transistor network with a p-MOS pull-up network simply means connecting a p-MOS transistor with gate grounded as load device. The circuit is now named as pseudo n-MOS gate since it is derived from n-MOS technology. However, this circuit requires the condition of $\beta_n > \beta_p$. Otherwise, low $V_{OL}$ value is difficult to achieve. The most significant disadvantage of using a pseudo n-MOS gate is non-zero static power dissipation since the always switched on p-MOS transistor is consuming power when the output is a logic 0.

Let’s consider a pseudo n-MOS inverter circuit shown in Fig. 5.24(a) and its corresponding voltage transfer characteristic shown in Fig. 5.24(b).

![Diagram of pseudo n-MOS inverter](image)

**Figure 5.24:** (a) A pseudo n-MOS inverter and (b) The voltage transfer characteristic of the inverter.

For the p-MOS transistor, the source-to-drain voltage $V_{SDp}$ is equal to $V_{SDp} = V_{DD} - V_{out}$ and source-to-gate voltage $V_{SGp}$ is equal to $V_{DD}$. For the n-MOS transistor, the gate-to-source voltage $V_{GSn}$ is equal to $V_{in}$ and the drain-to-source voltage $V_{DSn}$ is equal to $V_{out}$. For input $V_{in}$ equal to $V_{DD}$, $V_{out}$ is equal to $V_{OL}$, thus, $V_{GSn} = V_{DD}$ and $V_{SDn} = V_{OL}$. This is a clear indication that the n-MOS transistor is in linear mode. For the p-MOS transistor, $V_{SDp} = V_{DD} - V_{OL}$ and $V_{SGp} = V_{DD}$. This is an indication that the p-MOS transistor is in saturation mode if $V_{OL} < |V_{tp}|$. Equating the drain current flowed from p-MOS transistor to n-MOS transistor would obtain equation (5.13).
\[
\frac{\beta_n}{2} [2(V_{DD} - V_{in})V_{OL} - V_{OL}^2] = \frac{\beta_p}{2} (V_{DD} - |V_{tp}|)^2
\]

which indicates that for low \( V_{OL} \), condition \( \beta_n > \beta_p \) is required. The sheet resistance of the \( p \)-MOS transistor is about 2.5 times higher than the sheet resistance of the \( n \)-MOS transistor. As the rule of thumb, the resistance value of \( p \)-MOS transistor should be 5 times the resistance value of \( n \)-MOS transistor. This shall mean \((L/W)_p = 2(L/W)_n\). This implies that \((W/L)_n = 2(W/L)_p\).

The layout of a complex logic circuit function \((A \cdot B) + C\) design with pseudo \( n \)-MOS gate is shown in Fig. 5.25. Notice that the dimension of the \( n \)-MOS transistor network is two times larger than the grounded \( p \)-MOS transistor.

**Figure 5.25:** Layout of a complex logic function \((A \cdot B) + C\) designed with pseudo \( n \)-MOS gate design concept

One of the popular applications of pseudo \( n \)-MOS logic gate is the implementation of programmable logic array PLA. This device is originally
created for standalone device that allows user to program for different functionality. The capability of PLA is limited and has been replaced by significantly more powerful field programmable gate arrays FPGA. Designer usually likes to develop PLA into a highly regular, multiple output structure for the ease of automatic layout generation. Indeed ROM is also designed using this concept.

The block of a PLA is shown in Fig. 5.26. It consists of an input buffer that provides both non-inverting and inverting input and a two-level combinational circuits that provide sum-of-product SOP logic functions. The “AND” block is responsible for generate product term and the “OR” is responsible for selection of product term to form the desire logic output.

![Figure 5.26: The block diagram of a PLA](image)

The design examples of logic circuit using PLA is shown in Fig. 5.27.
The circuit consists of a 2-input AND gate, a 2-input NOR gate, and an exclusive OR gate. The input buffer provides the inverting and non-inverting logic, which are A, B, \(A\), and \(B\). The row provides the product term. Row 1 shows the pseudo n-MOS \(A+B\) gate, which is also the product term \(\overline{A} \cdot \overline{B}\). Row 2 shows the pseudo n-MOS \(A + \overline{B}\) gate, which is also the product term \(\overline{A} \cdot \overline{B}\). Row 3 shows the pseudo n-MOS \(\overline{A} + B\) gate, which is also the product term \(A \cdot B\). Row 4 shows the pseudo n-MOS \(\overline{A} + B\) gate. Column 1 has a pseudo n-MOS inverter, whereby its input is connected to \(A + B\), which will yield \((A+B)\). However, after connected to an inverter, it yield back \(A+B\) logic. Column 2 has the input of the pseudo n-MOS inverter connected to \((A \cdot B)\), which will result \(\overline{A} \cdot B\). However, after the inverter, it yields \((A \cdot B)\) logic. Column 3 has a 2-input pseudo n-MOS NOR gate, whereby its inputs are respectively connected to \(A \cdot B\) and \(A \cdot \overline{B}\), which would result exclusive NOR gate. However, after the inverter, it yields back exclusive OR logic.

**Figure 5.27:** The design of logic circuit using PLA
5.6 Transmission Gate

A CMOS transmission gate TG is designed by connecting an n-MOS and a p-MOS transistor in parallel as shown in Fig. 5.28.

![Circuit schematic](a) (b) (c)

Figure 5.28: CMOS transmission gate

The transmission gate is controlled by the signal S. Logic 1 connected to signal pin S switches on the n-MOS transistor, whilst logic 0 means \( \bar{S} \) switches the p-MOS transistor. The transmission gate acts as a good electrical switch connecting between X input and Y output. The transmission gate can transmit the entire logic 0 voltage, which is \( V_{SS} \) voltage and logic 1, which is \( V_{DD} \) voltage. P-MOS transistor is used to transmit logic 1 since it can pass strong logic 1, whilst n-MOS transistor is used to transmit logic 0 since it can pass strong logic 0. The transmission gate TG is classified as bi-directional type, whereby Fig. 5.28(b) shows the meaning. The back-to-back arrow indicating that the data can flow in either direction. The symbol in Fig. 5.28(c) is another representation of transmission gate showing data X is transfer to Y output.

5.6.1 Electrical Characteristics

The electrical characteristics of transmission gate shall be discussed in this section. Let’s examine transmitting logic 1 and logic 0 voltages through a transmission gate that has a capacitive load as shown in the circuit of Fig. 5.29. The input voltage is assumed to be at \( V_{DD} \), whilst the output voltage is taken across the capacitor. It is assumed that both transistors are biased into conduction with \( V_{DD} \) voltage applied to the gate of the n-MOS transistor, and 0V applied to the gate of the p-MOS transistor. Using KCL, the output node as
shown gives rise to the equation for output voltage. The complicating factor in solving this equation is depending upon the conduction states of MOS transistor change as the output capacitor is charged or discharged. To understand the behavior of the transmission gate, we will separately study the cases for which correspond respectively to transferring logic 1 through the transmission gate TG and followed by logic 0 transfer.

5.6.1.1 Transfer Logic 1

The transfer of logic 1 is shown in Fig. 5.29 whereby the input X is set at \( V_{DD} \) and the output Y is \( V_{out} \) with initial condition at 0V. The flow of current is from left to right.

![Figure 5.29: The condition of transmission gate for input X = V_{DD}](image)

The drain-to-source voltage of \( n \)-MOS transistor \( V_{DSn} = V_{DD} - V_{out} \), whilst the gate-to-source voltage is equal to \( V_{GSn} = V_{DD} - V_{out} \). Thus, the \( n \)-MOS transistor is at saturation mode at time \( t = 0 \) and it will not in linear mode through the transfer. The \( n \)-MOS transistor is in switched off mode if \( V_{GSn} < V_{tn} \), which is \( V_{DD} - V_{out} < V_{tn} \). This shall mean that the \( n \)-MOS transistor is in switched-off mode when \( V_{out} > V_{DD} - V_{tn} \). Since after switched-off, the transistor will be at saturation mode, thus, the \( n \)-MOS transistor will be in saturation mode if \( V_{out} < V_{DD} - V_{tn} \).

The drain-to-source voltage of \( p \)-MOS transistor is \( V_{DSP} = V_{out} - V_{DD} \), whilst the source-to-gate voltage \( V_{SGp} = -V_{DD} \). The \( p \)-MOS transistor is in saturation mode when \( V_{DSP} > V_{GSp} - |V_{tp}| \), which is \( V_{out} - V_{DD} > -V_{DD} - |V_{tp}| \). Thus, the \( p \)-MOS transistor will be linear mode \( V_{out} > |V_{tp}| \). The \( p \)-MOS transistor will be
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switched mode if \( V_{GSp} < |V_{tp}| \). This implies that \( |V_{tp}| > V_{DD} \), which cannot be happened. Therefore, the \( p \)-MOS transistor is never in switched-off mode.

Since \( V_{out} \) voltage is gradually increased from 0V to \( V_{DD} \), one can see that the \( n \)-MOS transistor is changing from saturation mode to cut-off mode when \( V_{out} > V_{DD} - V_{in} \). The \( p \)-MOS transistor changes from saturation mode to linear mode when \( V_{out} > |V_{tp}| \).

The analysis also shows that there are three operating regions for the transmission gate. The first region both \( n \)-MOS and \( p \)-MOS transistors are in saturation mode until the \( V_{out} \) is equal to \( |V_{tp}| \). The second region is for \( V_{out} \) ranges from \( V_{tp} \) to \( (V_{DD} - V_{in}) \). In this region, the \( n \)-MOS transistor is in saturation and \( p \)-MOS transistor is in linear region. The third region is for \( V_{out} \) ranges from \( (V_{DD} - V_{in}) \) to \( V_{DD} \). In this region, the \( n \)-MOS transistor is in cut-off mode and \( p \)-MOS transistor is in linear mode.

The channel resistance for various regions can be analyzed based on the equation for channel resistance, which is \( R_{p,n} = \frac{V_{DS,p,n}}{I_{D,p,n}} \). In third region, only \( p \)-MOS transistor is in linear region, therefore, the channel resistance \( R_p \) is

\[
R_p = \frac{2}{\beta [2(V_{DD} - V_{tp}) - (V_{DD} - V_{out})]} \tag{5.14}
\]

Student is encouraged to derive the channel resistance of the transmission gate for region I and II.

Figure 5.30 summaries the mode state of the \( n \)-MOS and \( p \)-MOS transistors during the output transition from 0V to \( V_{DD} \).
5.6.1.2 Transfer Logic 0

The transfer of logic 0 can be analyzed with the aid of Fig. 5.31, where the flow of current is from right to left side of the transmission gate. The drain-to-source voltage of the n-MOS transistor is $V_{DSn} = V_{out}$, whilst the gate-to-source voltage is equal to $V_{GSn} = V_{DD}$. Thus, the n-MOS transistor is in saturation mode at time $t = 0$. This shall mean that the n-MOS transistor is in saturation mode if $V_{out} > V_{DD} - V_{tn}$. The n-MOS transistor will be in linear mode if $V_{out} < V_{DD} - V_{tn}$. The n-MOS transistor is in switched-off mode if $V_{GSn} < V_{tn}$, which is $V_{DD} < V_{tn}$. This cannot be happened. Thus, the n-MOS transistor is never in switched-off mode during the logic 0 transfers.

The drain-to-source voltage of p-MOS transistor is $V_{DSP} = -V_{out}$, whilst the gate-to-source voltage $V_{GSp} = -V_{DD}$. Thus, the p-MOS transistor is in saturation mode at time $t = 0$. The p-MOS transistor is in saturation mode when $V_{DSP} > V_{GSp} - |V_{tp}|$, which is $-V_{out} > -V_{DD} - |V_{tp}|$. This implies that $V_{out} < V_{DD} + |V_{tp}|$. If the p-MOS transistor is in linear mode, this means that $V_{out} > V_{DD} + |V_{tp}|$, in which it cannot be happened. Thus, the p-MOS transistor is never in linear mode during the transfer of logic 0. The p-MOS transistor is in cut-off mode when $V_{GSp} < |V_{tp}|$, which is $V_{out} < |V_{tp}|$. 

![Diagram showing mode conditions of n-MOS and p-MOS transistors](image-url)
Figure 5.31: The condition of transmission gate for input $X = 0$ V

Since $V_{\text{out}}$ voltage is gradually decreased from $V_{\text{DD}}$ to 0V, this draws the conclusion that there are three operating regions for the transmission gate. The first region both $n$-MOS and $p$-MOS transistors are in saturation mode until the $V_{\text{out}}$ is equal to $(V_{\text{DD}} - V_{tn})$. The second region is for $V_{\text{out}}$ ranges from $(V_{\text{DD}} - V_{tn})$ to $V_{tp}$. In this region, the $p$-MOS transistor is in saturation and $n$-MOS transistor is in linear region. The third region is for $V_{\text{out}}$ ranges from $V_{tp}$ to 0. In this region the $p$-MOS transistor is in cut-off mode and $n$-MOS transistor is in linear mode.

In third region, only $n$-MOS transistor is operating in linear region, therefore, the channel resistance $R_n$ is

$$R_n = \frac{2}{\beta[2(V_{\text{DD}} - V_{tn}) - (V_{\text{out}})]} \quad (5.15)$$

Figure 5.32 summaries that mode state of the $n$-MOS and $p$-MOS transistors during the output transition from $V_{\text{DD}}$ to 0V.
5.6.2 RC Model of Transmission Gate

The RC model of a transmission gate is shown in Fig.5.33. The capacitance of input side is denoted as $C_X$ and the output side is denoted as $C_Y$. $R_{TG}$ denotes resistance of the transmission gate. $S$ denotes input to gate of $n$-channel MOS transistor of transmission gate, where the transistor is switched on. $\overline{S}$ input to $n$-channel MOS transistor means the transmission gate is switched off.

![Diagram of RC model of a transmission gate]

**Figure 5.33:** RC model of a transmission gate with input node $X$ and output node $Y$

The input to the transmission is a step function $V_{in}(t) = V_{DD}u(t)$ for transfer from a logic 0 to logic 1. The output voltage $V_{out}(t)$ is seen as the charging of capacitance $C_{out}$, which is comprised of $C_Y$ and the load capacitance $C_{Load}$.
through resistance of transmission gate $R_{TG}$. Thus, the $V_{out}(t)$ is equal to $V_{out}(t) = V_{DD}[1-\exp(-t/\tau_{TG})]$. $C_Y$ is equal to $C_{GSn}+K_n(0,V_{DD})C_{SBn}+C_{GDp}+K_p(0,V_{DD})C_{DBp}$.

For a transfer of logic 1 to logic 0, the $V_{in}(t)$ is $V_{in}(t) = V_{DD}[1-u(t)]$. The output voltage $V_{out}(t)$ is seeing discharging of through $R_{TG}$ and $C_{out}$. Thus, the output voltage $V_{out}(t)$ is $V_{out}(t) = V_{DD}\exp(-t/\tau_{TG})$. Note that $u(t) = 0$ for $t = 0$ and $u(t) = 1$ for $t \neq 0$.

The resistance of the transmission gate $R_{TG}$ is generally calculated using equation (5.16).

$$R_{TG} = \frac{V_{TG}}{I_{Dp} + I_{Dn}}$$

(5.16)

It is also equal to the parallel channel resistance of $n$-channel and $p$-channel MOS transistors. Depending on the condition of the logic transfer, the resistance of the transmission can be varied. Figure 5.34 shows the resistance of the transmission gate with various output voltage $V_{out}$ condition for logic 1 transfer.

![Figure 5.34: The $R_{TG}$ of a transmission gate with logic 1 transfer](image)

Figure 5.35 shows the resistance of the transmission gate with various output voltage $V_{out}$ condition for logic 0 transfer.
5.6.3 Application of Transmission Gate

Let’s study the application of transmission gate in designing the logic circuits i.e. both the combinational and sequential circuits. Since transmission gate is made of a pair of $n$-MOS transistor and $p$-MOS transistor with complimentary gate control, thus a gate control $A$ is split into $A = (A \cdot 1 + \overline{A} \cdot 0)$, where $A \cdot 1$ is used to control $n$-MOS transistor and $\overline{A} \cdot 0$ is used to control $p$-MOS transistor.

The switching characteristic of transmission gate is particularly useful for designing multiplexer MUX circuit. The Boolean function of the 2-to-1 multiplexer is $F = \overline{S} \cdot P_0 + S \cdot P_1$. Based on the function $F$, logic of $P_0$ is passed through the transmission gate when selected $S$ is asserted low. Thus, when $S$ is at logic 0 and $\overline{S}$ is at logic 1, the logic of $P_0$ is passed. Likewise, when $S$ is at logic 1 and $\overline{S}$ is at logic 0, the logic of $P_1$ is passed. The function equation of the multiplexer can also be written as $F = P_0(\overline{S} \cdot 1 + S \cdot 0) + P_1(S \cdot 1 + \overline{S} \cdot 0)$, where the term in parenthesis corresponds to logic control of transmission gate. $P_0(\overline{S} \cdot 1 + S \cdot 0)$ indicates that $\overline{S}$ is connected to $n$-MOS transistor and $S$ is connected to $p$-MOS transfer, while $P_0$ is connected in series with the transmission gate. $P_1(S \cdot 1 + \overline{S} \cdot 0)$ indicates that $\overline{S}$ is connected to $p$-MOS transistor and $S$ is connected to $n$-MOS
transfer, while \( P_1 \) is connected in series with the transmission gate. The logic circuit of 2-to-1 multiplexer is shown in Fig. 5.36.

\[
\text{Figure 5.36: A 2-to-1 multiplexer circuit}
\]

The Boolean function of exclusive-NOR gate is
\[
f(A, B) = \overline{A} \oplus B = A \cdot B + A \cdot \overline{B}.
\]
The function can also be written as
\[
f(A, B) = \overline{A} \cdot (B \cdot 1 + B \cdot 0) + A \cdot (B \cdot 1 + \overline{B} \cdot 0)
\]
 taking \( B \) as the control bit. This shall mean that input \( \overline{A} \) is true only if \( p \)-MOS transistor controlled by bit \( B \) is true and \( A \) is true only if \( p \)-MOS transistor controlled by bit \( \overline{B} \) is true. The detailed circuit is shown in Fig. 5.37.

\[
\text{Figure 5.37: CMOS circuit of a 2-input exclusive-NOR gate}
\]

The function of the exclusive OR gate can also be written as
\[
f(A, B) = \overline{A} \cdot B + A \cdot \overline{B} = \overline{A} \cdot (B \cdot 1 + B \cdot 0) + A \cdot (B \cdot 1 + B \cdot 0)
\]
. The exclusive-OR gate design using transmission gate is shown in Fig. 5.38.
The Boolean function of a two-input OR gate is \( f(A, B) = A + B = \overline{A} \cdot \overline{B} \cdot 0 + \overline{A} \cdot B \cdot 1 + A \cdot \overline{B} \cdot 1 + A \cdot B \cdot 1 = \overline{A} \cdot \overline{B} \cdot 0 + A \cdot 1 + B \cdot 1 = B \cdot \overline{A} + A \cdot \overline{A} \). Since the function \( f(A, B) \) of OR gate is \( A + B \), this function can also be written as \( \overline{A} \cdot B + A = B \cdot (A \cdot 1 + A \cdot 0) + A \cdot (A \cdot 1 + \overline{A} \cdot 0) \). The first term corresponds to a transmission gate with \( B \) as input and \( A \) as control.

The second term corresponds to either a \( p \)-MOS with \( A \) as input and \( \overline{A} \) as control or an \( n \)-MOS with \( A \) as input and \( A \) as control. Note that logic function \( A \cdot \overline{A} \cdot 1 \) always provides either open circuit or logic 1, which is an indication of OR B circuit. The CMOS circuit of the two circuit of two-input OR gate designed using transmission gate and either \( p \)-MOS or \( n \)-MOS is shown in Fig. 5.39.
The Boolean function of a two-input AND gate is \( f(A, B) = A \cdot B = A \cdot (B \cdot 1 + B \cdot 0) + B \cdot (B \cdot 0 + B \cdot 1) \). \( A \cdot (B \cdot 1 + B \cdot 0) \) indicates that \( B \) is connected to the gate of \( n \)-MOS transistor of the transmission gate, while \( \overline{B} \) is connected to the \( p \)-MOS transistor of the transmission gate. \( A \) is connected in series with the transmission gate. \( B \cdot (B \cdot 0 + \overline{B} \cdot 1) \) indicates that \( B \) is connected to the gate of \( p \)-MOS transistor of the transmission gate, while \( \overline{B} \) is connected to the \( n \)-MOS transistor of the transmission gate. \( B \) is connected in series with the transmission gate. Since \( B \) is connected to transmission gate that is control by \( B \) or \( \overline{B} \). Therefore, one of the transistors of the second part of the transmission is sufficient to provide the necessary logic state. Moreover, \( B \cdot \overline{B} \) provides logic 0, when input \( B \) is at logic 0, otherwise the output will be undefined high impedance state. The logic circuit of the AND gate is shown in Fig. 5.40.
5.7 Domino Logic Circuit

Domino CMOS logic circuit is an extension of dynamic logic circuit by adding in an inverter to prevent possibility of \textit{n}-MOS-\textit{n}-MOS transistor glitch. The general domino logic circuit is shown in Fig. 5.41.

When timing signal $\phi$ is at logic 0, the capacitor C is pre-charged to voltage $V_{DD}$. The output shall be at logic 0. When timing signal $\phi$ is at logic 1, the domino circuit is in evaluation mode. Depending on the condition of the \textit{n}-MOS transistor network, the charge in the capacitor may maintain to provide logic 0 at output or discharge through the \textit{n}-MOS transistor network to provide logic 1 at output. Based on the circuit design, domino logic never provides inverting logic at the output.

![Figure 5.41: General circuit of domino circuit design](image)

Domino circuit is always used in cascade design. The output of each stage is connected to a MOS transistor in next stage and the output of the later stage is then connected to a MOS transistor in the forward stage and so on. The example of the domino logic circuit of Boolean function of a three input OR gate is shown in Fig. 5.42.
Since charge leakage problem can lead to error, this problem can be overcome by adding in the charge keeper $p$-MOS transistor $M_{p1}$ as shown in the domino 3 input OR gate design in Fig. 5.43. If there is any leakage of the capacitor $C$ after the pre-charge stage, the charge keeper $p$-MOS transistor $M_{p1}$ will be able to restore the charge of the capacitor $C$ since it is always in the switched-on mode.

Another improve version of the charge keeper circuit is shown in Fig. 5.44. The charge keeper $p$-MOS transistor is biased by the output of the circuit. If the output is at logic 0, it switches-on the charge keeper $p$-MOS transistor and restores the charge due to leakage in the capacitor $C$. If the output is at logic 1 the charge keeper transistor is in switched-off mode. It also shows that the
evaluated result is logic 0, which shall mean that the capacitance should lose all the charges.

**Figure 5.44:** Domino circuit of a 3-input OR gate with feedback control to charge keeper $p$-MOS transistor

In order to prevent from the parasitic effect, an extra inverter $Z$ can be added as feedback to the charge keeper $p$-MOS transistor $M_{p1}$. It also frees the output from slowdown due to induced flipping state of the feedback network. The 3 input OR gate domino circuit with the feedback inverter is shown in Fig. 5.45.

**Figure 5.45:** A domino 3-input OR gate with inverter feedback to charge keeper $p$-MOS transistor
5.8 Transistor Level Design of Flip-Flop

Flip-flop is the primitive memory element, which is shown in Fig. 5.46. It contains two NOT gates where the outputs are fed to inputs of the opposite NOT gate. The CMOS circuit of the bi-stable element is shown in Fig. 5.47.

![Figure 5.46: A basic bi-stable element](image)

When logic 1 is connected to input A, the output Q is at logic 0. The logic state is input to second NOT gate and its output \( \overline{Q} \) will be at logic 1, which is the same state as the input A. In this manner, the output Q and \( \overline{Q} \) would stay at its respective logic state even if the logic 1 at input A is removed.

![Figure 5.47: CMOS circuit of a bi-stable element](image)

When logic 0 is connected to input A, the output Q will be at logic 1. The logic state is input to second NOT gate and its output \( \overline{Q} \) will be at logic 0, which is
the same state as the input A. In this manner, the output \( Q \) and \( \bar{Q} \) would remain at its respective logic state even if the logic 0 at input A is removed. Combining both conditions of logic states, the bi-stable element forms the basic memory bit. The layout of the bi-stable element is shown in Fig. 5.49.

The bi-state element has two stable states and one unstable state. The unstable state occurs at the mid-point voltage. At this point all transistors are in saturation mode and also at the highest potential energy.

The SR flip-flop is shown in Fig. 5.50. The output \( \bar{Q} \) is \( \bar{Q} = S \cdot \text{CLK} + Q \) and \( Q = R \cdot \text{CLK} + \bar{Q} \). Using DeMorgan’s theorem, \( \bar{Q} \) is also equal to \( \bar{Q} = (S + \text{CLK}) \cdot \bar{Q} \), which forms the p-MOS transistor circuit of the output \( \bar{Q} \). Output \( Q \) is also equal to \( (R + \text{CLK}) \cdot \bar{Q} \), which forms the p-MOS transistor circuit of output \( Q \).
Based on \( p \)-MOS and \( n \)-MOS transistors’ equations of the SR flip-flop, the CMOS circuit design of the SR flip-flop is shown in Fig. 5.51.

The D flip-flop is shown in Fig. 5.52. The output \( \overline{Q} \) is \( \overline{Q} = \overline{D + Q} = \overline{D} \cdot \overline{Q} \), whilst the output \( Q \) is \( Q = \overline{\overline{Q} + D} = \overline{Q} \cdot \overline{D} \).
The CMOS circuit of the D flip-flop shall be as shown in Fig. 5.53.

The transmission gate design of a basic D flip-flop is shown in Figure 5.54. During the load operation, Load = 1 with D = 1, the first transmission gate is switched on, while the second transmission gate is off. During the hold operation whereby Load = 0, the first transmission gate is off, while the second transmission gate is switched on. Thus, the data D = 1 is maintained at Q output. The node X has logic function \( D \cdot Load \). The feedback to node X has logic function \( (D \cdot Load) \cdot Load \), which logic 0. This has no bearing effect at node X in which it still has logic function \( D \cdot Load \) maintained.
Another compact way to design a D flip-flop is shown in Fig. 5.55. The output at node X is $D \cdot Load + \overline{D} \cdot \overline{Load}$, which is equal to $D$. Thus, data $D$ is latched when $Load$ is equal to logic 1.

In order to avoid wrong data being latch into the D flip-flop, the D flip-flop can be designed with master/slave operation that utilizing transmission gate and NOT gates. Figure 5.56 shows the CMOS design of a master/slave D flip-flop.
Transmission gate B and D are used to prevent the output of master flip-flop and slave flip-flop from driving the output of transmission gate A and C. Unless the output of transmission gate A and C is able to sink or source sufficient current to overcome the output drive from output of master flip-flop and slave flip-flop, wrong data latch would occur. Besides having transmission gate B and D, the aspect ratio W/L of transmission gate A and C can be designed sufficient large as compare with the aspect ratio of other transistor.

At node X, the logic function is $\text{Load} \cdot \overline{D}$ and the logic function at node Y is $\overline{\text{Load}} \cdot D$. The logic function at node Y is $\overline{\text{Load}} \cdot D \cdot \text{Load} = (\overline{\text{Load}} \cdot D) + \text{Load}$ and the logic function at node Z is $(\overline{\text{Load}} \cdot D) + \text{Load} = D$, which is the data D.

**Figure 5.56**: A master/slave D flip-flop

The JK flip-flop is shown Fig. 5.57. The Boolean function of output $\overline{Q}$ is $\overline{Q} = \overline{Q} \cdot \overline{J} \cdot \overline{CLK} + Q$, which is also equal to $(\overline{Q} + \overline{J} + \overline{CLK}) \cdot Q$. The Boolean function of $Q$ is $Q = Q \cdot \overline{K} \cdot \overline{CLK} + \overline{Q}$, which is also equal to $(\overline{Q} + \overline{K} + \overline{CLK}) \cdot \overline{Q}$. 
Based on the output equations mentioned above, the CMOS circuit design of the JK flip-flop is shown in Fig. 5.58.

The T flip-flop is shown in Fig. 5.59. The Boolean function of output $\overline{Q}$ is $\overline{Q} = \overline{Q} \cdot T \cdot \overline{CLK} + Q = (\overline{Q} + \overline{T} + \overline{CLK}) \cdot \overline{Q}$ and the Boolean function of output $Q$ is $Q = Q \cdot T \cdot CLK + \overline{Q} = (Q + \overline{T} + CLK) \cdot \overline{Q}$.
Based on the output equations, the CMOS circuit design of the T flip-flop is shown in Fig. 5.60.

5.9 Random Access Memory Devices

In this section the designs of static RAM, dynamic RAM, and ROM will be discusses. The block diagram of a 1kx8 SRAM is shown in Fig. 5.61.
This memory device has 128 row addresses and 8 column addresses. The memory has 8 matrix blocks and each block has 128x8 cells. The other main parts of the memory are the sense amplifier, control unit, input/output data control, output data control, address bus, and data bus.

We shall discuss the approaches used to design memory cell – static and dynamic cell, the sense amplifier, and the address decoders – row and column decoders, and I/O data control circuits.

5.9.1 RAM Memory Cell

There are many methods to design the static and dynamic random access memory cells. In this section, three methods are presented. They are six-transistor static memory cell, three-transistor dynamic memory cell, and one-transistor dynamic memory cell.
5.9.1.1 Six-Transistor Static Memory Cell

The six-transistor static memory cell is shown in Fig. 5.62. MOS transistors $M_1$, $M_2$, $M_3$, and $M_4$ form the bi-stable memory element, whilst $n$-MOS transistors $M_5$ and $M_6$ are served as pass-transistors.

![Figure 5.62: The six-transistor static RAM cell](image)

During the write cycle, the desired logics are placed on bit line and $\overline{\text{BIT}}$ line. When the WORD line is asserted, the desired data will be latched into the bi-stable memory element. For an example, to write logic 1 into the memory, the BIT line is set at logic 1, whilst the $\overline{\text{BIT}}$ line is at logic 0.

However, due to high pack density of the memory cell whereby many column memory cells are connected in the same bit line, the total drain-bulk capacitance of the pass-transistors is sufficiently large that the charging and discharging of the bit lines would take long time. Thus, during the read cycle, the BIT and $\overline{\text{BIT}}$ lines are pre-charged to the pre-defined level, which is usually 0.5 of $V_{DD}$ voltage level. These lines are then allowed to float. When the WORD line is asserted, the BIT line and $\overline{\text{BIT}}$ line begin to charge or discharge that reflect the logic level stored in memory cell. The small change in voltage level is passed to the sense amplifier for output user. The read cycle is a destructive cycle whereby the data stored in the memory can be erased. Therefore, it is necessary to refresh the memory. Other mean to prevent the bit data being erased is to design the pass-transistor to have large width and length. But this is not desired because in the modern design, scale down is necessary to save cost and fast access time.
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5.9.1.2 Three-Transistor Dynamic Memory Cell

The three-transistor dynamic RAM structure is shown in Fig. 5.63. Transistor $M_1$ is used to write the BIT logic into the source of transistor $M_1$ and gate of transistor $M_2$. With the present of source capacitance $C_S$, depending on the logic being written, the gate voltage of transistor $M_2$ is either at logic 0 or logic 1 that has voltage $(V_{DD} - V_{tn(M2)})$ due to threshold loss.

![Figure 5.63: A three-transistor dynamic RAM cell](image)

The BIT value is logic 0 then the gate voltage shall be 0V. If the BIT value is at logic 1 then the gate voltage will be at logic 1 that has voltage $(V_{Write} - V_{tn(M2)})$. This voltage is held on as long as the Read transistor $M_3$ is not switched on.

During the read cycle, transistor $M_3$ is switched on and if the BIT value is logic 1 then the $\overline{BIT}$ line would turn logic 0. Likewise, if the BIT value is logic 0 then upon reading the $\overline{BIT}$ line would turn to logic 1 that has maximum value $(V_{Read} - V_{tn(M3)})$. 

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5.9.1.3 One-Transistor Dynamic Memory Cell

One-transistor dynamic RAM cell uses capacitor to temporarily store the charge on a memory capacitor $C_M$. A simple 1-bit dynamic RAM cell is shown in Fig. 5.64.

During the write cycle, the logic level is placed on the BIT line. The WORD line is then asserted to charge or discharge the memory capacitor $C_M$. The capacitor is leaky and will not hold the charge for long time. Thus, it is necessary to refresh it periodically.

During the read cycle, the BIT line is pre-charged and placed in tri-state mode. When the WORD line is asserted, the BIT capacitor $C_{BIT}$ is either charging or discharging depending on the charge stored in memory capacitor $C_M$. The sense amplifier is then used to detect small change in voltage level and output the appropriate logic level.

Read cycle is a destructive operation. Thus, the data must be re-written into the memory capacitor $C_M$.

5.10 dc Characteristic of a NOT Gate

When the input of an inverter is biased with voltage $V_{in}$, the output would respond with voltage $V_{out}$. The gate-to-source voltages of the inverter as shown in Fig. 5.65 are $V_{GSp} = |V_{DD} - V_{in}|$ and $V_{GSn} = V_{in}$. Depending on the voltage
value of $V_{\text{in}}$ which can be ranged from 0 to $V_{\text{DD}}$ volt, the minimum and maximum values of the $V_{\text{GSp}}$ are 0 and $V_{\text{DD}}$ respectively. Similarly, $V_{\text{GSn}}$ also has the same minimum and maximum values.

When the value of either $V_{\text{GSn}}$ or $|V_{\text{GSp}}|$ is increased from 0V to $V_{\text{DD}}$ volt, the state of $n$-MOS transistor and $p$-MOS transistor moved from cut-off to saturation region and then move into linear region. This is clearly demonstrated when the value of $V_{\text{GSn}}$ or $V_{\text{GSp}}$ are less than the value of $V_{\text{in}}$ or $|V_{\text{tp}}|$, the transistors are in cut-off state. When the values of $V_{\text{GSn}}$ or $V_{\text{GSp}}$ are greater than the value of $V_{\text{in}}$ or $|V_{\text{tp}}|$, the transistors move into saturation region. This is because $V_{\text{DS}}$ of transistor is greater the value of $(V_{\text{GSn}} - v_{\text{tn}})$ or $(V_{\text{GSp}} - |V_{\text{tp}}|)$. The transistors finally move to linear state when the values of $(V_{\text{GSn}} - v_{\text{tn}})$ or $(V_{\text{GSp}} - |V_{\text{tp}}|)$ are greater than $V_{\text{DS}}$.

The voltage transfer characteristic VTC of a NOT gate or inverter is shown in Fig. 5.66. It is a plot of output voltage $V_{\text{out}}$ versus input voltage $V_{\text{in}}$. When the input voltage is $V_{\text{DD}}$, the output voltage $V_{\text{out}}$ will swing to 0V, which is $V_{\text{OL}} = 0V$. When input voltage $V_{\text{in}}$ is set at 0V, the output will swing to $V_{\text{DD}}$, which is $V_{\text{OH}}$ and it is equal to $V_{\text{DD}}$.

![Diagram of an inverter or NOT gate]

**Figure 5.65:** The voltage bias condition of an inverter or NOT gate

The voltage transfer characteristic VTC of an inverter has three distinct regions; the low input region where $V_{\text{in}} < V_{\text{IL}}$, the transition region where $V_{\text{IL}} \leq V_{\text{in}} \leq V_{\text{IH}}$, and the high input region $V_{\text{in}} > V_{\text{IH}}$. The output has two transitions, one at $V_{\text{in}} = V_{\text{IL}}$ and one at $V_{\text{in}} = V_{\text{IH}}$. The transition is defined as the region between point 2 and 4 where the slope = -1.
Figure 5.66: The transient response of a NOT gate

$V_{OH}$ is the minimum output voltage that will establish a high-level logic 1. $V_{OL}$ is the maximum output voltage that will establish a low-level logic 0. $V_{IL}$ is the maximum positive voltage that can be applied to an input terminal of a gate and still be recognized as logic 0. $V_{IH}$ is the minimum positive voltage that can be applied to an input terminal of a gate and still be recognized as logic 1.

In transition region, the output is undefined. The width of the transition region $V_{TW}$ is a measure of ambiguity and is defined as

$$V_{TW} = V_{IH} - V_{IL} \quad (5.17)$$

A low $V_{TW}$ is desirable to reduce ambiguity in the input logic-state. Logic swing $V_{LS}$ is also a measure of ambiguity in logic-state and is defined as

$$V_{LS} = V_{OH} - V_{OL} \quad (5.18)$$

A high value of $V_{LS}$ is desirable to reduce ambiguity and increase noise immunity.

The noise margin of the device is divided into two types namely noise margin for logic 1, which $V_{NM_H} = V_{OH} - V_{IH}$ and noise margin for logic 0, which is $V_{NM_L} = V_{IL} - V_{OL}$.
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At point 1, the \( p \)-MOS transistor is in ohmic region and \( n \)-MOS transistor is at cut-off region. This region corresponds to output at logic 1.

At point 2, it is the region where the gradient of the VTC is -1. This is the point that the input low voltage \( V_{IL} \) and output high voltage \( V_{OH} \) can be determined. Based on the condition at this point, saturation current of \( n \)-MOS transistor is equal to linear current of \( p \)-MOS transistor. Thus,

\[
\frac{\beta_n}{2} (V_{in} - V_{in})^2 = \frac{\beta_p}{2} [2(V_{DD} - V_{in} - |V_{tp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2]
\]

(5.19)

To derive \( \frac{dV_{out}}{dV_{in}} = -1 \), one needs to perform partial differentiation at both sides of equation (5.19), which is dependent on \( V_{in} \) at left-hand side and dependent on \( V_{in} \) and \( V_{out} \) at right-hand side. Thus,

\[
\frac{dI_{Dn}}{dV_{in}} dV_{in} + \frac{\partial I_{Dp}}{\partial V_{in}} dV_{in} + \frac{\partial I_{Dp}}{\partial V_{out}} dV_{out} = \frac{\partial I_{Dn}}{\partial V_{in}} dV_{in} - \frac{\partial I_{Dp}}{\partial V_{out}} dV_{out}
\]

(5.20)

Rearranging equation (5.20), it yields equation (5.21).

\[
\frac{dV_{out}}{dV_{in}} = \frac{\frac{dI_{Dn}}{dV_{in}} - \frac{\partial I_{Dp}}{\partial V_{in}}}{\frac{\partial I_{Dp}}{\partial V_{out}}} = -1
\]

(5.21)

Substituting the derivative, it yields equation (5.22), which is

\[
V_{in} \left(1 + \frac{\beta_n}{\beta_p}\right) = 2V_{out} - V_{DD} - |V_{tp}| + \frac{\beta_n}{\beta_p} V_{in}
\]

(5.22)

One may take equation (5.19) and (5.22) to solve for two unknowns, which are \( V_{in} = V_{IL} \) and \( V_{out} = V_{OH} \) respectively.

Point 3 is the mid-point voltage point, where the input voltage \( V_{in} \) is equal to output voltage \( V_{out} \). At mid-point voltage \( V_{M} \) or switching voltage, both \( n \)-MOS and \( p \)-MOS transistors are in saturation mode. The mid-point voltage \( V_{M} \) can be derived by equating the saturation current of the \( p \)-MOS and the \( n \)-MOS
transistors, and setting output voltage $V_{\text{out}} = V_M$, which is

$$\frac{\beta_p}{2} (V_{\text{DD}} - V_M - |V_{\text{tp}}|)^2 = \frac{\beta_n}{2} (V_M - V_{\text{tn}})^2.$$ 

This yields equation (5.23).

From equation (5.23), it shows that the mid-point voltage $V_M$ is determined by

$$V_M = \frac{V_{\text{DD}} - |V_{\text{tp}}| + \sqrt{\beta_n V_{\text{tn}}}}{1 + \sqrt{\beta_n / \beta_p}}$$

(5.23)

Knowing that the mobility of $n$-MOS transistor is 2 to 3 times higher than the mobility of $p$-MOS transistor, therefore, the aspect ratio of $p$-MOS transistor should be 2 to 3 times larger than the aspect ratio of $n$-MOS transistor for obtaining symmetrical inverter VTC.

At point 4, the $p$-MOS transistor is in saturation region and $n$-MOS transistor is in linear region. This point corresponds to the end of transition and output begins to go to logic 0. This is the region where the gradient of the VTC is also equal to -1, where the input high voltage $V_{\text{IH}}$ and actual output low voltage $V_{\text{OL}}$ can be determined. Based on the condition at this point saturation $p$-MOS transistor current is equal to linear $n$-MOS transistor current. Thus,

$$\frac{\beta_p}{2} (V_{\text{DD}} - V_{\text{tn}} - |V_{\text{tp}}|)^2 = \frac{\beta_n}{2} [2(V_{\text{in}} - V_{\text{tn}})V_{\text{out}}^2]$$

(5.24)

To derive $\frac{dV_{\text{out}}}{dV_{\text{in}}} = -1$, one needs to partial differentiation both sides of equation (5.19), which dependent on voltage $V_{\text{in}}$ at left-hand side and dependent on $V_{\text{in}}$ and $V_{\text{out}}$ at right-hand side. Thus,
\[
\frac{dI_{Ip}}{dV_{in}} \cdot dV_{in} = \frac{\partial I_{Dn}}{\partial V_{in}} \cdot dV_{in} + \frac{\partial I_{Dn}}{\partial V_{out}} \cdot dV_{out} \tag{5.25}
\]

Rearranging equation (5.25), it yields equation (5.26).

\[
\frac{dV_{out}}{dV_{in}} = -1
\]  
\[
\frac{\partial I_{Dn}}{\partial V_{in}} \tag{5.26}
\]

Substituting the derivative into equation (5.26), it yields equation (5.27).

\[
V_{in} \left(1 + \frac{\beta_{p}}{\beta_{n}}\right) = 2V_{out} + V_{in} + \frac{\beta_{p}}{\beta_{n}} \left(V_{DD} - |V_{IP}|\right) \tag{5.27}
\]

One may take equation (5.24) and (5.27) to solve for two unknowns, which are  
\[V_{in} = V_{IH} \text{ and } V_{out} = V_{OL} \text{ respectively.}\]

In region 5, the \(p\)-MOS transistor is in cut-off region, whilst the \(n\)-MOS transistor is in ohmic region. This is the region where the output is at logic 0.

### 5.11 ac Characteristics of a NOT Gate

The ac characteristic of a NOT gate, which is its switching waveform, is shown in Fig. 5.67. \(t_f\) is the fall time and \(t_r\) is the rise time. The output does not respond immediately upon changing the input voltage because there is capacitance and resistance associated with the inverter whereby the charging and discharging of the capacitance cause the delay of response at the output.
The RC model of the NOT gate is shown in Fig. 5.68. $R_p$ and $R_n$ are the channel resistances of the $p$-MOS and $n$-MOS transistors, which can be calculated from the ohmic equation of the MOS transistor by assuming the largest possible gate-to-source voltage $V_{GS}$ be equal to $V_{DD}$. Thus, the channel resistance is $R_n = \frac{\eta}{\beta_n (V_{DD} - V_{tn})}$, where $\eta$ ranges from 1 to 6 depending on technology. For simplicity $\eta$ is equal to 1. Applying $\eta = 1$ to the channel resistance of the $n$-MOS and $p$-MOS transistors respectively, they become

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{tn})} \quad (5.28)$$

$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{tp}|)} \quad (5.29)$$

$R_{sn}$ and $R_{sp}$ are sheet resistances of $n$-MOS and $p$-MOS transistor respectively. For 0.12µm and $V_{DD} = 1.2$V technology, the sheet resistances are respectively equal to $R_{sn} = 1.8k\Omega/\square$ and $R_{sp} = 5.5k\Omega/\square$ respectively.
\( C_{Dp} \) and \( C_{Dn} \) are the total diffusion capacitance of \( p \)-MOS and \( n \)-MOS transistors that were defined earlier. They are defined as

\[
C_{Dp} = C_{GSp} + C_{DBp} = \frac{1}{2} C_{ox} LW_p + C_{jp}(WX)_p + C_{jwp}(2W + 2X)_p \quad (5.30)
\]

\[
C_{Dn} = C_{GSn} + C_{DBn} = \frac{1}{2} C_{ox} LW_n + C_{jn}(WX)_n + C_{jwn}(2W + 2X)_n \quad (5.31)
\]

As for the diffusion capacitance values of sidewall and bottom of drain, what are specified in equation (5.30) and (5.31) are maximum values, which do not include the variation due to biasing of the substrate and switching event. The precise way is to include the linear time-invariant LTI factor. LTI factors for the sidewall and bottom capacitance are respectively equal to equation (5.32) and (5.33).

\[
K_{1/3}(0, V_{DD}) = \frac{3V_{biw}}{2V_{DD}} \left[ \frac{V_{DD}}{V_{biw}} \right]^{2/3} - 1 \quad (5.32)
\]

and
The sum of drain capacitance of \( n \)-MOS and \( p \)-MOS transistors is termed as capacitance of NOT gate \( C_{\text{FET}} \) or it can be called as internal capacitance of the NOT gate. Thus,

\[
C_{\text{FET}} = C_{\text{int}} = C_{Dn} + C_{Dp} \tag{5.34}
\]

The load capacitance \( C_L \) is depending on the number of gate driven by the inverter and the line capacitance \( C_{\text{metal}} \) of the metal interconnect, which is defined in equation (10.4). Therefore, the load capacitance \( C_L \) is equal to

\[
C_L = FO(C_{Gn} + C_{Gp}) + C_{\text{metal}} \tag{5.35}
\]

where \( FO \) is the fan-out value.

The total output capacitance \( C_{\text{out}} \) of the NOT gate is now equal to the sum of capacitance \( C_{\text{FET}} \) and the load capacitance \( C_L \), which is

\[
C_{\text{out}} = C_{\text{FET}} + C_L \tag{5.36}
\]

If the inverter drives three NOT gates then the load capacitance \( C_L \) is equal to \( 3(C_{Gn} + C_{Gp}) \) plus metal interconnect capacitance \( C_{\text{metal}} \), where \( C_{Gn} \) and \( C_{Gp} \) are the gate capacitance of the \( n \)-MOS and \( p \)-MOS transistors of the circuit driven by the inverter. Note that in this case, the Fan-out value \( FO \) is equal to three.

### 5.11.1 Fall Time of NOT Gate

The discharge time of the NOT gate is defined as the time taken for the output of the NOT gate to fall from logic 1 to logic 0 through resistance \( R_n \). Initially the output voltage is at \( V_{\text{DD}} \) and is discharged to zero volt though the switched-on resistance of the \( n \)-MOS transistor. It follows the normal capacitor discharge equation, which is

\[
V_{\text{out}} = V_{\text{DD}} \exp(-t/\tau_n) \tag{5.37}
\]

where \( \tau_n \) is the time constant, which is equal to \( C_{\text{out}} R_n \). Rewriting equation (5.37) as time \( t \), it yields equation (5.38).
The fall time $t_f$ is defined as the time taken for the output to fall from 90% of its maximum output value to 10% of its maximum output value. Thus, fall time $t_f$ is equal to

$$t_f = \tau_n \ln \frac{V_{DD}}{0.1V_{DD}} - \tau_n \ln \frac{V_{DD}}{0.9V_{DD}} = \tau_n \ln(9) = 2.2\tau_n$$

The fall time is $t_f = 2.2\tau_n = 2.2(R_nC_{out}) = \frac{2.2C_{out}}{\beta_n(V_{DD} - V_{tn})}$. Since $V_{DD} >> V_{tn}$, therefore, the fall time $t_f$ can be estimated as $t_f = \frac{2.2C_{out}}{\beta_n V_{DD}}$. The fall time $t_f$ is also known as $t_{HL}$ transition time.

### 5.11.2 Rise Time of NOT gate

The charging time of the NOT gate is time taken for the output of the NOT gate to rise from logic 0 to logic 1 voltage through resistance $R_p$. Initially, the output voltage is at zero volt and is charged to $V_{DD}$ volt through the switched-on resistance of the $p$-MOS transistor, which follows the normal capacitor charging equation, which is

$$V_{out} = V_{DD} [1 - \exp(-t/\tau_p)]$$

where $\tau_p$ is the time constant equals to $C_{out}R_p$. Rewriting equation (5.40) as time $t$, it yields equation (5.41).

$$t_r = \tau_p \ln \frac{V_{DD}}{V_{DD} - V_{out}}$$

The rise time $t_r$ is defined as the time taken for the output to rise from 10% of its maximum output value to 90% of its maximum output value. Thus, rise time $t_r$ is equal to

$$t_r = \tau_p \ln \frac{V_{DD}}{V_{DD} - 0.9V_{DD}} - \tau_p \ln \frac{V_{DD}}{V_{DD} - 0.1V_{DD}} = \tau_p \ln(9) = 2.2\tau_p$$
The rise time is 

\[ t_r = 2.2 \tau_p = 2.2(R_p C_{out}) = \frac{2.2 C_{out}}{\beta_p (V_{DD} - |V_{tp}|)} \]  

Since \( V_{DD} >> |V_{tp}| \), therefore, the rise time \( t_r \) can be estimated to be equal to 

\[ t_r = \frac{2.2 C_{out}}{\beta_p V_{DD}}. \] 

The fall time \( t_f \) is known as \( t_{HL} \) time, the high-to-low transition time since it is the time taken to transit from logic 1 to logic 0. Similarly, the rise time \( t_r \) is also known as \( t_{LH} \), the low-to-high transition time since it is the time taken for the output to transit from logic 0 to logic 1.

The reciprocal of the sum of fall time \( t_f \) and rise time \( t_r \) is a time value used to determine the maximum operating frequency \( f_{max} \) of the NOT gate, which is shown in equation (5.43).

\[ f_{max} = \frac{1}{t_f + t_r} \]  

Knowing that time constant \( \tau_n = R_n C_{out} \), \( \tau_p = R_p C_{out} \) and total capacitance \( C_{out} = C_{FET} + C_L \), the fall time \( t_f \) and rise time \( t_r \) are arranged respectively equal to 

\[ t_f = 2.2 \tau_n = 2.2 R_n (C_{FET} + C_L) = t_{f0} + \alpha_p C_L \]  

(5.44) 

\[ t_r = 2.2 \tau_p = 2.2 R_p (C_{FET} + C_L) = t_{r0} + \alpha_n C_L \]  

(5.45) 

where \( t_{f0} = 2.2 R_n C_{FET} \) and \( t_{r0} = 2.2 R_p C_{FET} \) are design dependent values. \( \alpha_p \) and \( \alpha_n \) are respectively equal to \( \alpha_p = 2.2 R_p \) and \( \alpha_n = 2.2 R_n \). From equation (5.44) and (5.45), one can see that the fall time \( t_f \) and rise time \( t_r \) of the NOT gate are dependent on the external load capacitance \( C_L \).

5.11.3 Propagation Delay Time of NOT Gate

Propagation delay time \( t_p \) is often used to estimate the “reaction” delay time from input to output. When step-like input voltage is used, propagation delay time \( t_p \) is defined as 

\[ t_p = \frac{t_{nf} + t_{pf}}{2} \]  

(5.46) 

where \( t_{nf} \) is the time taken for the output to fall from its maximum output voltage to 50% of its maximum output voltage. Thus, from equation (5.38), \( t_{nf} \) is
equal to $\tau_n \ln(2)$. $T_{pr}$ is the time taken for the output to rise from zero volt to 50% of its maximum output voltage. From equation (5.41), $t_{pr}$ is equal to $\tau_p \ln(2)$. Based on the above analysis, the propagation delay time $t_p$ is equal to

$$t_p = \frac{\ln 2}{2} (\tau_n + \tau_p)$$  \hspace{1cm} (5.47)

Knowing that $\tau_n = R_n C_{out}$, $\tau_p = R_p C_{out}$ and $C_{out} = C_{FET} + C_L$, equation (5.47) shall be

$$t_p = \frac{\ln 2}{2} (C_{FET} + C_L)(R_n + R_p)$$ \hspace{1cm} (5.48)

From equation (5.48), one can see that the propagation delay time $t_p$ of the NOT is dependent on the load capacitance $C_L$, which has the same conclusion as shown by equation (5.44) and (5.45) for fall time and rise time.

**5.12 Electrical Analysis of NAND Gate**

The transistor level circuit of a NAND gate is shown in Fig. 5.69. Since the device has two inputs, it implies that the NAND has more than one voltage transfer characteristic curve VTC. As the results, there are three different mid-point voltage $V_M$ depending on the transition state.

![Figure 5.69: The transistor level circuit of a NAND gate](image-url)
According to the truth table, there is only input state that the output is at logic 0 and the other three input states that output is at logic 1. Thus, we shall look at transition from logic 1 to logic 0 for output. This also implies that there is a state of simultaneous transition of the input from both logic 0 state to logic 1 state. The other two states are caused by change of either one of the input state. The detail of the logic state transition of the NAND and conditions of transistor are shown in Fig. 5.70.

Transition (i) is a simultaneous transition where both input A and B are changing logic state from logic 0 to logic 1. During this transition both transistor $M_1$ and $M_2$ switch from on-state to off-state, while transistor $M_3$ and $M_4$ switch from off-state to on-state.

Transistor $M_1$ and $M_2$ are connected in parallel. During on-state, the transistor $M_1$ and $M_2$ can be treated as one transistor having width of 2$W$ instead $W$. Thus, the device transconductance is equal to $2\beta_p$.

Based on this analytical approach, one can get a generalized equation to represent the equivalent device transconductance $\beta_{eq}$ for $n$ parallel connected MOS transistors, which is shown in equation (5.49).

$$\frac{1}{\beta_{eq}} = \frac{1}{\beta_1 + \beta_2 + \ldots + \beta_n}$$

(5.49)

Alternatively, equation (5.49) can be written in terms of device’s aspect ratio $W/L$, which is equation (5.50).

$$\frac{L_{eq}}{W_{eq}} = \frac{1}{W_1/L_1 + W_2/L_2 + \ldots + W_n/L_n}$$

(5.50)
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The transistor $M_3$ and $M_4$ are connected in series. During on-state, transistor $M_3$ and $M_4$ can be treated as one transistor having channel length of $2L$ instead $L$. Thus, the device transconductance is equal to $\beta_n/2$.

Based on this analytical approach, one can get a generalized equation to represent the equivalent device transconductance $\beta_{eq}$ for $n$ series connected MOSFETs, which is shown in equation (5.51).

$$\frac{1}{\beta_{eq}} = \frac{1}{\beta_1} + \frac{1}{\beta_2} + \ldots + \frac{1}{\beta_n}$$ (5.51)

Alternatively, equation (5.51) can be written in terms of device’s aspect ratio $W/L$, which is equation (5.52).

$$\frac{L_{eq}}{W_{eq}} = \frac{L_1}{W_1} + \frac{L_2}{W_2} + \ldots + \frac{L_n}{W_n}$$ (5.52)

Based on the similar approach, the analysis is similar for the transition from logic 1 to logic 0. This shall also mean that for simultaneous transition, the NAND gate can be treated as inverter that has device transconductance parameter $2\beta_p$ and $\beta_n/2$ respectively for $p$-MOS and $n$-MOS transistors. From the mid-point voltage or inversion threshold voltage equation (5.23), the mid-point voltage of NAND gate during simultaneous input transition is

$$V_M = \frac{V_{DD} - |V_{tp}| + \frac{\beta_n / 2}{2\beta_p}V_{tn}}{1 + \frac{\beta_n / 2}{2\beta_p}}$$ (5.53)

The result shows that there is a shift of inversion threshold voltage $V_M$ toward the right side of inverter’s VTC curve since $V_M$ value is larger.

Consider the NAND gate transistor circuit shown in Fig. 5.71, the output capacitance $C_{out}$ is equal to $C_{FET} + C_{L}$, where $C_{FET}$ is equal to $C_{Dn} + 2C_{Dp}$ and $C_{L}$ is the load capacitance.

The reason that $C_{FET}$ is equal to $C_{Dn} + 2C_{Dp}$ is based on worst case scenario. Since transistor $M_1$ and $M_2$ are connected in parallel, the worst case capacitance is $2C_{Dp}$. Since transistor $M_3$ and $M_4$ are connected in series than the worst case capacitance is $C_{Dn}$. 
From equation (5.28) and (5.29), the channel resistances of \( n \)-MOS and \( p \)-MOS transistors are respectively equal to

\[
R_n = \frac{1}{\beta_n (V_{DD} - V_m)} \quad \text{and} \quad R_p = \frac{1}{\beta_p (V_{DD} - |V_m|)}.
\]

\[ \text{Figure 5.71: NAND circuit for transient response calculation} \]

During the charging phase, \( C_{out} \) capacitance is charged from 0 volt to \( V_{DD} \) volt. The output voltage \( V_{out} \) is equal to

\[
V_{out} = V_{DD} \left[ 1 - \exp\left(-t/\tau_p\right) \right] \quad (5.54)
\]

The time constant \( \tau_p \) is equal to \( R_p C_{out} \), which has the worst case \( R_p \) resistance. Since rise time \( t_r \) is defined as time taken for \( V_{out} \) to rise from \( 0.1V_{DD} \) to \( 0.9V_{DD} \), therefore, the rise time \( t_r \) is equal to \( t_r = 2.2\tau_p \). This equation can be written as

\[
t_r = 2.2R_p(C_{FET} + C_L) \quad (5.55)
\]

or

\[
t_r = 2.2R_p(C_{FET} + C_L) = t_0 + \alpha_0 C_L \quad (5.56)
\]

where \( t_0 = 2.2R_pC_{FET} \) is the non load rise time and \( \alpha_0 \) is equal to \( 2.2R_p \). If both \( M_1 \) and \( M_2 \) transistors are conducting then the channel resistance should be
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Rp/2. This would give a best case scenario since $\tau_p$ in this case is half of the previous case.

During the discharging of $C_{out}$ capacitance discharges from $V_{DD}$ volt to 0 volt, the output voltage $V_{out}$ is equal to

$$V_{out} = V_{DD}\exp(-t/\tau_n)$$  \hspace{1cm} (5.57)

According to circuit shown in Fig. 5.70, the time constant $\tau_n$ is given by $\tau_n = 2R_nC_{out} + R_nC_X$. $C_X$ is the inter transistor capacitance of n-MOS transistor, which is usually equal to sum of $C_{Dn}$ of transistor $M_4$ and $C_{Sn}$ of transistor $M_3$. One can view it from the layout of the series transistors. The fall time $t_f$ is then given by

$$t_f = 2.2\tau_n = 2.2[2R_nC_{out} + R_nC_X]$$  \hspace{1cm} (5.58)

or

$$t_f = 2.2\tau_n = t_1 + \alpha_1C_L$$  \hspace{1cm} (5.59)

where $t_1 = 2.2R_n(2C_{FET} + C_X)$ and $\alpha_1 = 4.4R_n$.

5.12 Electrical Analysis of NOR Gate

The transistor level circuit of a NOR gate is shown in Fig. 5.72. Since the device has two inputs, it implies that the NOR gate has more than one voltage transfer characteristic curve VTC. Indeed, there are three different mid-point voltage $V_M$ depending on the transition state.

According to the truth table, there is only input state that the output is at logic 1 and the other three input states that output is at logic 0. Thus, we shall look at transition from logic 0 to logic 1 for output. This also implies that there is a state of simultaneous transition of the input from both logic 1 state to logic 0 state. The other two states are caused by change of either one of the input state. The detail of the logic state transition of the NOR and conditions of transistor are shown in Fig. 5.73.

Transition (i) is a simultaneous transition where both input A and B are changing logic state from logic 1 to logic 0. During this transition both transistor $M_1$ and $M_2$ switch from off-state to on-state, while transistor $M_3$ and $M_4$ switch from on-state to off-state.
Transistor $M_1$ and $M_2$ are connected in series. During on-state, the transistor $M_1$ and $M_2$ can be treated as one transistor having channel length of $2L$ instead $L$. Thus, the device transconductance is equal to $\beta_p/2$. Alternatively, equation (5.51) can be used to calculate the equivalent device transconductance.

Transistor $M_3$ and $M_4$ are connected in parallel. During on-state, transistor $M_3$ and $M_4$ can be treated as one transistor having width of $2W$ instead $W$. Thus, the device transconductance is equal to $2\beta_n$. Alternatively, equation (5.49) can be used to calculate the equivalent device transconductance.

Based on the similar approach, the analysis is similar for the transition from logic 0 to logic 1. This shall also mean that for simultaneous transition, the
NOR gate can be treated as inverter that has device transconductance parameter $\frac{\beta_p}{2}$ and $2\beta_n$ respectively for $p$-MOS and $n$-MOS transistors. From mid-point voltage equation (5.23), the mid-point voltage of NOR gate during simultaneous input transition is

$$V_M = \frac{V_{DD} - |V_{ip}| + \frac{2\beta_n}{\sqrt{\beta_p/2}}V_{in}}{1 + \frac{2\beta_n}{\sqrt{\beta_p/2}}} \quad (5.60)$$

The result shows that there is a shift of $V_M$ toward the left side of inverter’s VTC curve since $V_M$ is smaller.

The graphs in Fig. 5.75 show the plots of voltage characteristic curves for NOR gate, NAND gate, and NOT gate.

Consider the NOR gate transistor circuit shown in Fig. 5.75, the output capacitance $C_{out}$ is equal to $C_{out} = C_{FET} + C_L$, where $C_{FET}$ is equal to $2C_{Dn} + C_{Dp}$ and $C_L$ is the load capacitance.
The reason that $C_{FET}$ is equal to $2C_{Dn} + C_{Dp}$ is based on worst case scenario. Since transistor $M_3$ and $M_4$ are connected in parallel, the worst case capacitance is $2C_{Dn}$. Since transistor $M_1$ and $M_2$ are connected in series than the worst case capacitance is $C_{Dp}$.

The channel resistances of $n$-MOS and $p$-MOS transistors are respectively equal to $R_n = \frac{1}{\beta_n (V_{DD} - V_m)}$ and $R_p = \frac{1}{\beta_p (V_{DD} - |V_{pp}|)}$.

During the charging of $C_{out}$ capacitance charges from 0 volt to $V_{DD}$ volt, the output voltage $V_{out}$ is equal to

$$V_{out} = V_{DD}[1 - \exp(-t/\tau_p)] \quad (5.61)$$

The time constant $\tau_p$ is equal to $2R_p C_{out} + R_p C_Y$, which has the worst case channel resistance equal to $2R_p$. $C_Y$ is the inter transistor capacitance of $p$-MOS transistor. $C_Y$ is usually equal to the sum of $C_{Dp}$ of transistor $M_1$ and $C_{Sp}$ of transistor $M_2$. Thus, the $t_r$ rise time is

$$t_r = 2.2R_p(2C_{FET} + C_Y + 2C_L) \quad (5.62)$$

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or

\[ t_f = 2.2R_p(2C_{\text{FET}} + C_Y + 2C_L) = t_0 + \alpha_0C_L \] (5.63)

where \( t_0 = 2.2R_p(2C_{\text{FET}} + C_Y) \) is the non load rise time and \( \alpha_0 \) is equal to 4.4\( R_p \).

During the discharging of \( C_{\text{out}} \) capacitance discharges from \( V_{DD} \) volt to 0 volt, the output voltage \( V_{out} \) is equal to

\[ V_{out} = V_{DD}\exp(-t/\tau_n) \] (5.64)

According to circuit shown in Fig. 5.75, the time constant \( \tau_n \) is given by \( \tau_n = R_n C_{out} \). The fall time \( t_f \) is then given by

\[ t_f = 2.2\tau_n = 2.2R_nC_{out} \] (5.65)

or

\[ t_f = 2.2\tau_n = t_1 + \alpha_1C_L \] (5.66)

where \( t_1 = 2.2R_nC_{\text{FET}} \) and \( \alpha_1 = 2.2R_n \).

5.13 Power Dissipation of NOT Gate

The power dissipation of the NOT gate shall be analyzed in this Section. There are two types of power dissipation associated with CMOS circuit. They are static power dissipation \( P_{DC} \) and dynamic power dissipation \( P_{dyn} \). When the circuit is not in operation the power dissipation is known as static power dissipation \( P_{DC} \). When it is in operation, it is known as dynamic power dissipation \( P_{dyn} \). Thus, for a NOT gate, the static power dissipation is equal to \( P_{DC} = V_{DD}I_{DDQ} \). Based on the voltage characteristic curve shown in Fig. 5.66 and the drain current plot shown in Fig. 5.76, the output of the NOT gate is either at logic 1 or logic 0, whereby in both cases, one of the MOS transistor is at cutoff. Since the \( p \)-MOS transistor is connected in series with \( n \)-MOS transistor, theoretically, there is no power dissipation at static condition. However, due to sub-threshold conduction and other leakage associated with the design, there is a small amount of current in pico-ampere per gate. This current is termed as quiescent leakage current \( I_{DDQ} \). Thus, static power dissipation is \( P_{DC} = V_{DD}I_{DDQ} \). One has to take note that during the transition of the output voltage either changing from logic 1 to logic 0 or from logic 0 to logic 1, the maximum dc current consumption occurred when output voltage is equal to input voltage,
which is the mid-point voltage $V_M$ of Fig. 5.76 at point 3. At this point, both $p$-MOS and $n$-MOS transistors are in saturation mode. It is obvious to say the maximum current drain occurred when both $n$-MOS and $p$-MOS transistors are connected in series are in saturation mode. The dynamic power dissipation $P_{\text{dyn}}$ can be calculated with the charging and discharging figure shown in Fig. 5.77.

The output is charged to $V_{\text{DD}}$ during transition to logic 1 and discharged to logic 0 during transition to logic 0. The sum of charging and discharging time is considered as equal to the period $T$ of the input frequency. Thus, the dynamic current $i_{\text{DD}}$ is equal to $Q/T$, where $Q$ is the charge of output capacitor $C_{\text{out}}$, which is also equal to $V_{\text{DD}}C_{\text{out}}$. The dynamic power $P_{\text{dyn}}$ is equal to

$$P_{\text{dyn}} = V_{\text{DD}}i_{\text{DD}} = V_{\text{DD}} \frac{Q}{T} = C_{\text{out}} V_{\text{DD}}^2 f$$  \hspace{1cm} (5.67)
After adding the static power $P_{DC}$, the total power dissipation $P_D$ of the NOT gate is

$$P_D = V_{DD}I_{DDQ} + C_{out} V_{DD}^2 f$$  \hspace{1cm} (5.68)

### 5.14 Power Dissipation of Complex Logic Gate

The total power dissipation $P_D$ of the logic gate is $P_D = V_{DD}I_{DDQ} + C_{out} V_{DD}^2 f$ after ignoring the short circuit power dissipation. Since the static power $V_{DD}I_{DDQ}$ is small as compared to the dynamic power. Therefore, power dissipation of logic gate is basically come from dynamic power. Dynamic power is power consumption resulted from transistor switching from logic 0 to logic 1 and from logic 1 to logic 0. For a complex logic circuit that has many transitions and if we assume that there are equal chance of transition from logic 0 to logic 1 and vice versa, then we can introduce the term activity coefficient $a$, which is the product of probability $p_0$ of transition from logic 0 to logic 1 and $p_1$ the probability of transition from logic 1 to logic 0. Thus, activity coefficient is $a = p_0 p_1$. The power dissipation of a gate can be written as

$$P_D = aC_{out} V_{DD}^2 f$$  \hspace{1cm} (5.69)

Take for an example, a 2-input NOR has three logic 0 output and one logic 1 output, the activity coefficient is $a = \frac{3}{4} \cdot \frac{1}{4} = \frac{3}{16}$. However, most of the digital system shows that the maximum activity coefficient is 0.5. Thus, in general equation (5.69) can be re-written as

$$P_{dyn} = 0.5C_{out} V_{DD}^2 f$$  \hspace{1cm} (5.70)

For a complex circuit that contains $N$ complex gate, the total power dissipation after ignoring static power dissipation is equal to

$$P_D = \sum_{i=1}^{N} a_i C_i V_i V_{DD} f$$  \hspace{1cm} (5.71)

or

$$P_D = \sum_{i=1}^{N} 0.5C_i V_i V_{DD} f$$  \hspace{1cm} (5.72)
Exercises

5.1. A pseudo $n$-MOS transistor circuit is shown in figure below. Calculate the worst case aspect ratio of $p$-MOS transistor if the sheet resistance of $p$-MOS transistor is equal to 2.5 times of the sheet resistance of $n$-MOS transistor and the resistance value of $p$-MOS transistor should be 5 times the resistance value of $n$-MOS transistor.

![Circuit Diagram]

5.2. Design a logic function $f(A, B, C, D) = A + B + C$ using complimentary pass-transistor logic design concept.

5.3. The initial output condition of the transmission gate is 0V. Its input is then connected to $V_{DD}$. Calculate the channel resistance of the transmission gate when the output reaches $0.8V_{DD}$. Given that $V_{DD} = 3.0V$, the device’s transconductance $\beta = 1.5 \times 10^{-3}$S, and the threshold voltage of the MOSFET are $V_{tp} = |1.0V|$ and $V_{tn} = 1.0V$ respectively.

5.4. Consider an $n$-MOS pass-transistor that is connected as shown in figure with zero body bias threshold voltage $V_{tno} = 0.7V$, Fermi potential $\phi_F = 0.29V$, and bulk threshold parameter $\gamma = 0.053V^{1/2}$. With $V_{DD} = 3.3V$, find the maximum voltage that can be passed through this transistor.
5.5. Design a 4-to-1 MUX using transmission gate.

5.6. Design the transistor level circuit for a 1-to-4 de-multiplexer circuit.

5.7. Design an exclusive NOR gate using transmission gate.

5.8. From the circuit shown below, what is the logic function at output 1 and output 2?

5.9. Design a logic function \( f(A, B, C, D) = \overline{A \cdot B + C + D} \) with at least two transmission gates.

5.10. What is the difference between a combinational logic circuit and a sequential circuit?
5.11. Given a CMOS inverter has \( W_n = 20 \mu m,\ L_p = L_n = 2 \mu m,\ K_p = 2.0 \times 10^{-5} A/V^2,\ K_n = 5.0 \times 10^{-5} A/V^2,\) find the value of the gate width \( W_p\) for \( \beta_p = \beta_n.\)

5.12. Calculate the switching point of a CMOS inverter if \( \beta_n = 1.5 \beta_p,\ V_{tm} = |V_{tp}| = 0.7 V,\ V_{DD} = 5.0 V,\ K_n = 2.5 K_p,\ L_n = L_p = 1.0 \mu m.\)

5.13. Consider an \( n\)-MOS transistor that has a channel width \( W = 8 \mu m,\) a channel length of \( L = 0.5 \mu m\) and is made with a process where \( K_n = 180 \times 10^{-6} A/V^2,\ V_{tn} = 0.70 V\) and \( V_{DD} = 3.3 V.\) Calculate the channel resistance.

5.14. A complex CMOS logic function is \( f(A, B, C, D) = \overline{A} + B(C + D).\) Find the aspect ratio of each MOS transistor such that the gate delay is not worse than that of a basic CMOS inverter, which have aspect ratio 1.5 and 5 respectively for \( n\)-MOS and \( p\)-MOS transistor for 0.12\( \mu m\) technology.
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Bibliography