Chapter 2

UEEA3033
Microelectronics and
Semiconductor Materials

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Chapter 2

Device Fabrication

2.0 Introduction

Jack Kilby was the first person developed miniaturized transistor circuit in 1958. It was then followed by Robert Noyce and Gordon Moore, who built first planar miniaturized transistor in 1960. There after with the aid of computer and advancement in photolithography, integrated circuit IC was fast developed into ultra large scale integration ULSI where millions of transistors can be built in a silicon chip of 3.0cm x 3.0cm area.

Integrated circuit is mainly built on silicon due to cheap, developed processes, has stable silicon dioxide, and abandon on the earth crust. Beside these reasons, the by-product produced by the process is not toxic and can be disposed easily. There are many other available materials that can be used to build integrated circuit such GaAs, SiC, GaN, SiGe and etc. Unless, it is mentioned, this lecture shall be presented using silicon as the building element for the integrated circuit.

An integrated circuit IC consists of a single crystalline chip or it may be called monolithic, typically 300µm to 600µm thick and covering a surface area of 3.0cm x 3.0cm containing both active and passive elements. The process used to fabrication an IC covers wafer preparation, photolithography, epitaxial growth, impurity diffusion, ion implantation, oxidation, etching, metallization deposition, and annealing.

Today there are many developed fabrication technologies. These technologies are used to fabricate silicon and gallium arsenide based integrated circuit. Among the common types are the bipolar junction isolation JI, dielectric isolation DI, self align junction isolation SAJI, oxide isolation OI, vertical dual MOS, SiGe, complimentary metal oxide semiconductor CMOS, BiCMOS, self aligned double polysilicon, and etc.

2.1 Crystal Structure

The way atoms packed into solid material is important in electronic because it determines the electrical and physical properties of the solid material. Many
elements and compounds are crystalline, which shall mean the atoms are highly ordered packed together. The crystal structure of solid material is based on one type of lattice that it has three-dimensional grids where the atoms sit at the intersection of the grids. The simplest form of the lattice is the cube lattice, which is also called unit cell. It contains a group of atoms where it replicates the whole crystal structure. Figure 2.1 shows the unit cell and replica of the unit cell into a crystal lattice.

![Figure 2.1: Crystal lattice containing simplest dark-colored cube lattice](image)

Owing to the periodicity of lattice, it is useful to define the symmetry of the structure. The symmetry is defined via a set of point group operations, which involve a set of operations applied around a point. The operations involve rotation, reflection, and inversion.

Symmetry plays a very important role in electronic properties such as inversion symmetry. For example, diamond structure has inversion symmetry, thus, Si and Ge are not piezoelectric and do not have electro-optic effect. Semiconductor zinc blende crystal structures such as GaAs, InAs, and AlAs do not inversion symmetry. They have the properties of piezoelectric and electro-optic effect.

Rotation symmetry is another symmetry types. Lattices can have rotation symmetry of \(2\pi\), \(2\pi/3\), \(2\pi/4\), and \(2\pi/6\), which are denoted as 1, 3, 4, and 6. \(2\pi/5\) or \(2\pi/7\) is not allowed because it could not fill up an infinite space.

There are 14 types of lattice in 3-D. They are as follows.
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- 1 triclinic – with $a_1 \neq a_2 \neq a_3$ and $\alpha \neq \beta \neq \gamma$.
- 2 monoclinic – with $a_1 \neq a_2 \neq a_3$ and $\alpha = \gamma = 90^0 \neq \beta$.
- 4 orthorhombic – with $a_1 \neq a_2 \neq a_3$ and $\alpha = \beta = \gamma = 90^0$.
- 2 tetragonal - with $a_1 = a_2 \neq a_3$ and $\alpha = \beta = \gamma = 90^0$.
- 3 cube - with $a_1 = a_2 = a_3$ and $\alpha = \beta = \gamma = 90^0$.
- 1 trigonal - with $a_1 = a_2 = a_3$ and $\alpha = \beta = \gamma < 120^0$, $\neq 90^0$.
- 1 hexagonal - with $a_1 = a_2 \neq a_3$ and $\alpha = \beta = 90^0$, $\gamma = 120^0$.

where $a_1$ is the shortest period of the lattice. $a_2$ is the shortest period not parallel to $a_1$, and $a_3$ is the shortest period not coplanar with $a_1$ and $a_2$. $\alpha$, $\beta$, $\gamma$ are angles between them.

Semiconductor crystal lattice has cube structure. They are simple cube $sc$ as illustrated in Fig. 2.2(a), body-center cube $bcc$ as illustrated in Fig. 2.2(b), and face-centered cube $fcc$ as illustrated in Fig. 1.14(c).

![Figure 2.2](image)

**Figure 2.2:** (a) Simple cube, (b) body-centered cube, and (c) face-centered cubic crystals

Most semiconductors have very peculiar lattice structure, which consists of two interlocking face-centered cubic lattices, and have total of eight atoms per unit cell. This structure can be broken down into primitive cell of tetrahedral shape, which is shown in Fig. 2.3. Tetrahedral shape has volume $\left(\frac{a}{2}\right)^3$. A center atom at the center of tetrahedral structure, a distance $\frac{a}{4}$ away from the edge, forms four covalent bonds with for adjacent atoms at the corners. Figure 2.4 shows the diamond structure and Fig. 2.5 shows the zinc blende structure. Gallium arsenide GaAs has zinc blende structure which has gallium Ga at the center of tetrahedral and arsenic As at corners.
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Figure 2.3: Basic tetrahedral structure

Figure 2.4: Diamond structure

Figure 2.5: Zinc blende structure
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*a* is defined as lattice constant. It is the length between two atoms for a cubic unit cell. It is not necessary the smallest distance between two atoms.

### 2.2 Crystal Planes

It is useful to be able to refer to a particular plane within a crystal lattice because a particular plane has unique physical and electrical properties that may affect the design of electronic devices. For cubic cell, the three dimensional lattice points can be presented by the vector equation (2.1).

\[
r = pa + qb + sc
\]

(2.1)

Miller indices are integers, which represent one of the coordinates \(x, y, \text{ or } z\). The integers used are called *hkl*. Miller indices are found using the following procedures.

1. Find the intercepts on the axes represented by the basis vector \(a, b, c\) in terms of lattice constant \(a\).
2. Take the reciprocals of these numbers.
3. Reduce these three reciprocals to three integers having the same ratio, usually the smallest three integers.
4. These three new integers are Miller indices, represented by \(hkl\). The round bracket indicates that \(hkl\) denotes a plane.

Owing to symmetry of the unit cell, there are other equivalent crystal planes and it is denoted by \(\{hkl\}\).

The shaded areas of Fig. 2.5 and Fig. 2.6 have Miller indices 2, 3, 3 representing a (2, 3, 3) plane and 2, 0, 3 representing a (2, 0, 3) plane.

![Figure 2.5: Miller indices showing (2,3,3) plane](image)
Knowing the crystal plane, one also needs to know the crystal direction. The crystal direction is represented by \([h\ k\ l]\) and the equivalent plane is denoted by \(<h\ k\ l>\). Figure 2.7 illustrates the sample direction vectors and their corresponding Miller indices.

The most common two types of silicon crystal orientations used to fabricate the integrated circuit are (111) and (100) types. The selection of the type depends on the type circuit to be built. (111) orientation is widely used for fabricating bipolar device, whilst (100) type is mainly used to fabricate MOSFET. (100)-type has the surface state charge 30-40% less than (111) type. Thus, it is ideal to
use for MOSFET fabrication in which the device is sensitive to surface trapping and thereby affecting the mobility of the device. Bipolar device is a current driven device. Thus, the surface state charge would not have significant impact on the speed of the device. Moreover, choosing the right orientation would assist scribing in dicing of the silicon wafer. There are two type either \( p \) or \( n \) types and two common orientation types are being used in electronic device fabrication. The way to identify them is by mean of flat shown on the wafer. Figure 2.8 shows the flat used to identify orientation and dopant type of wafer.

\[
\begin{align*}
\text{(111) \( n \)-type} & \quad \text{(111) \( p \)-type} \\
\text{(100) \( n \)-type} & \quad \text{(100) \( p \)-type}
\end{align*}
\]

*Figure 2.8: Wafer flat for identifying the orientation and dopant type*

### 2.3 Crystal Defects

In a real crystal, the lattice is not perfect, but contains imperfections or defects. This shall mean that the periodicity of the crystal lattice is disrupted in some manners. Imperfection tends to alter the electrical properties especially when it contains impurity.

Thermal vibration of atom would cause the variation of inter-atomic distance. The type of imperfection is called *lattice vibration*. *Point defect* is caused by missing atom at a lattice location. An isolated vacancy in the lattice is termed a *Schottky defect*. The extra atom that causes disruption of the chemical
bonding between atoms is called *interstitial defect*. A vacancy associated with an interstitial atom i.e. associated vacancy–interstitial pair is referred to as a *Frenkel defect*.

Foreign atom or impurity may present in a crystal lattice. They are present as substitutional impurity or interstitial impurity. Foreign atom sites at a lattice location are called *substitutional impurity*. Foreign atom, which is sited in between lattice location, is called *interstitial impurity*. Figure 2.9 illustrates the type of crystal defects.

*Dislocation* is the defect that shows very significant effect on the electrical and optical behavior of the semiconductors. Dislocation interacts strongly with other defects. Fig. 2.10 shows two elementary types of dislocation, which are an *edge dislocation* and a *screw dislocation*. An edge dislocation can be described as the edge of an extra plane inserted into the crystal, whereas a screw dislocation introduces a helical distortion into the crystal. The presence of dislocations in terms of the type and distribution in crystalline semiconductors influences various properties like crystal growth process, mechanical strength, and electronic properties. Dislocations may be formed, when point defects aggregate at an atomic plane, or they can be introduced when the stress causes atomic planes to slip past each other at high temperatures during growth or processing. Owing to high energy, dislocation does not occur in thermodynamic equilibrium. Thus, large dislocation-free crystal such as Si has can be produced. The nature of a dislocation is specified by the *Burgers vector* \( \mathbf{b} \).
There are many other defects such as volume defect and surface that are not discussed here. Reader may refer to advanced book for details.

2.4 Crystal Growth

Before the fabrication of the integrated circuit, the preparation of silicon or gallium arsenide wafer is required. The preparation of wafer involves several process steps. They are distillation and reduction/synthesis, crystal growth, grind/saw/polish, and electrical and mechanical characterizations. We shall not discuss the process of making gallium arsenide GaAs wafer. We shall concentrate on the process of making silicon wafer.

The starting material is silicon dioxide for making silicon wafer. It is chemically processed to form a high-purity crystal polycrystalline semiconductor for which single crystal is formed. The single crystal ingot is shaped to define diameter and is sawed into wafer. The wafer is then etched and polished to provide smooth, specular surface where device is fabricated.

Pure form of sand SiO$_2$ called *quartzile* is placed in a furnace with various forms of carbon like coke, coal, and wood chip. Although there are numbers of reaction take place, the overall reaction follows equation (2.2).

$$\text{SiC} + \text{SiO}_2 \rightarrow \text{Si} + \text{SiO}↑ + \text{CO}↑$$

This process step produces metallurgical grade silicon with purity of about 98.0%. In next process step, the silicon is pulverized and treated with hydrochloric acid gas HCl at temperature 300°C to form trichlorosilane SiHCl$_3$. The chemical reaction follows equation (2.3).
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\[
\text{Si} + 3\text{HCl} \rightarrow \text{SiHCl}_3 + \text{H}_2↑ \tag{2.3}
\]

Trichlorosilane, a liquid at room temperature, with boiling point 320°C is fractional distilled to remove unwanted impurities. The purified SiHCl₃ is then used in the hydrogen reduction reaction to produce the electronic grade silicon EGS.

\[
\text{SiHCl}_3 + \text{H}_2 \rightarrow \text{Si} + 3\text{HCl}↑ \tag{2.4}
\]

The reaction takes place in a reactor containing resistance heated silicon rod, which serves as the nucleation point for deposition of EGS in polycrystalline form of high purity. This is the raw material used to prepare device quality single crystal. Pure EGS has impurity concentration generally in part per billion.

There are a number of methods used to prepare the crystalline ingot. We shall discuss two methods here namely Czochralski and Float-zone methods. Other methods such as horizontal zone furnace, which is Bridgeman-Stockbarger technique and Liquid encapsulated Czochralski LEC and etc are not discussed.

2.4.1 Czochralski Crystal Growth Method

The polycrystalline silicon is melt in the argon Ar atmosphere in quartz crucible. Right type and the amount of dopant is then added. With right temperature control and with the aid of “seed”, silicon rod of right diameter is formed by rotation and pulling in Czochralski puller as shown in Fig. 2.11. Figure 2.11(a) shows the photograph of a modern computer-controlled Czochralski crystal puller. Figure 2.11(b) is the schematic drawing showing the components of the puller.

Once thermal equilibrium is established, the temperature at the vicinity of the seed is reduced and the molten silicon begins to freeze out onto the seed crystal. Subsequently, the seed is slowly rotated and withdrawn at the rate of a few millimeter per minute to form a cylindrically shaped single crystal of silicon, which is known as ingot. Typically, 4 to 6 inch diameter and 1 to 2 meter in length type of ingot can be formed. In today’s process, ingot of diameter as large as 12 inches is commonly produced to save cost and improve productivity. However, for large ingot as large as 12 inches in diameter, an external magnetic field is applied around the crucible and it is used to control the concentration of defects, impurities, and oxygen.
In the crystal growth process, the most common dopants, which are boron and phosphorous, is used to make \( p \)- and \( n \)-type semiconductor materials respectively. As the crystal is pulled from the molten silicon, the doping concentration incorporated into the crystal is usually different from the doping concentration of the molten silicon at the interface. The ratio of these two concentrations is defined as the *equilibrium segregation coefficient* \( k_0 \), which is defined as

\[
k_0 = \frac{C_s}{C_l}
\]  

(2.5)

where \( C_s \) and \( C_l \) are respectively the equilibrium concentration of the dopant in the solid and liquid near interface. Figure 2.12 shows the equilibrium segregation coefficient for common dopants used for silicon. The value below one means that during the growth the dopants are rejected into the molten silicon. As the result, the dopant concentration of molten silicon becomes higher as time lapsed.
Consider a crystal being growth from the initial molten silicon of weight $M_o$ with an initial doping concentration $C_o$ (the weight of dopant per 1g of molten silicon) in the molten silicon. At a given time, a crystal of weight $M$ has been grown, the amount of the dopant remaining in the molten silicon by weight is $S$. For an incremental amount of the crystal with weight $dM$, the corresponding reduction of the dopant $-dS$ from the molten is $C_SdM$, where $C_S$ is the doping concentration in the crystal by weight.

$$-dS = C_SdM \quad (2.6)$$

The remaining weight of the molten silicon is $(M_o-M)$ and the doping concentration in liquid by weight $C_1$ is given by

$$C_1 = \frac{S}{M_o-M} \quad (2.7)$$

Substituting equation (2.6) and (2.7) into equation (2.5), it yields equation (2.8).

$$\frac{dS}{S} = -k_o \left( \frac{dM}{M_o-M} \right) \quad (2.8)$$

Given that the initial weight of the dopant $C_o M_o$, integration equation (2.8) yields equation (2.9).
Solving equation (2.9) and combining equation (2.7), it yields equation (2.10).

\[
C_S = k_0 C_o \left(1 - \frac{M}{M_o}\right)^{k_0 - 1}
\]  

(2.10)

During the growth of silicon ingot, dopant is constantly being rejected into the molten silicon. If the rejection rate is higher than the rate at which the dopant can be transported away by diffusion or stirring, then a concentration gradient will develop at the interface as shown in Fig. 2.13. The equilibrium segregation coefficient is \(k_0 = C_S/C_I(0)\). We can define an effective segregation coefficient \(k_e\), which is the ratio of \(C_S\) and the impurity concentration far away from the interface.

\[
k_e = \frac{C_S}{C_I}
\]  

(2.11)

Consider a small virtual stagnant molten layer of width \(\delta\) in which the only flow that required to replace the crystal being withdrawn from the molten. Outside the stagnant layer the concentration remains constant at \(C_I\). In the layer, the concentration can be described by steady state continuation equation.
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\[
D \frac{d^2C}{dx^2} + v \frac{dC}{dx} = 0
\]  

(2.12)

where \(D\) is the diffusion coefficient of the molten silicon and \(v\) is the velocity of the crystal growth. The solution of equation is \(C = A_1 e^{-\frac{vx}{D}} + A_2\) with the constant to be determined by two boundary conditions. The first is at \(x = 0, C = C_I(0)\) and second is determined by conservation of total number of dopant i.e. the sum of dopant flux at interface is zero. This condition yields equation.

\[
D \left( \frac{dC}{dx} \right)_{x=0} + [C_I(0) + C_S] = 0
\]  

(2.13)

Substituting the conditions and \(C = C_I\) at \(x = \delta\), the solution for the concentration \(C\) is

\[
e^{-\frac{v\delta}{D}} = \frac{C_I - C_S}{C_I(0) - C_S}
\]  

(2.14)

The effective segregation coefficient \(k_e\) is

\[
k_e = \frac{C_S}{C_I} = \frac{k_0}{k_0 + (1-k_0)e^{-\frac{v\delta}{D}}}
\]  

(2.15)

2.4.2 Float-Zone Crystal Growth Method

The float-zone crystal growth method is illustrated conceptually in Fig. 2.14. The crystal is not grown in the crucible that it has markedly reduced the impurity level particularly the level of oxygen. This method is used today for fabrication device that requires high resistivity and low oxygen content in the power device and detector device.

In the float-zone process, a polysilicon rod of EGS is clamped at both ends, with bottom in contact with a single-crystal seed. A small RF coil provides large current in silicon that locally melts the silicon. The molten zone is usually 2.0cm long. The liquid phase silicon is then bonded to the atomic plane of the seed plane by plane as the zone is slowly moved up. Doping of the crystal can be achieved by either starting with a doped polysilicon rod, a doped seed, or maintaining a gas ambient during the process that contains a dilute concentration of the desired dopant. As compared to Czochralski method, float-
zone method has a greater resistivity variation. Thus, Czochralski method is still the dominant method for large diameter silicon crystal.

![Diagram of float-zone crystal growth method]

**Figure 2.14:** Basic float-zone crystal growth method

### 2.5 Integrated Circuit Fabrication Process

Modern integrated circuit manufacturing facilities are designed to continuously re-circulate the room air through HEPA filters to maintain a class 10 or class 1 environment. A typical clean room is designed with all the mechanical support equipment such as pump is located beneath the clean room to minimize contamination. The HEPA filter is located in the ceiling of the clean room and the fans that re-circulate the air are normally above these filters. The finger wall or chases either at the wall or floor are used to provide return path of the air for recirculation.

People who are working in the area have to wear clean room attire to minimize contamination from particle emission of human being. Chemicals and gases used are electronic graded types and usually they are filtered on site prevent contamination.

De-ionized water is generated on site. De-ionized water or DI water is highly purified and filtered water that all traces of ionic, particles, and bacterial contamination have been removed. The theoretical resistivity of pure water at
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25°C is 18.3Mohm-cm. A basic DI water system can achieve resistivity of 18.0Mohm-cm with fewer than 1.2 colonies of bacteria per milliliter and no particle size larger than 0.25µm.

Ultra-clean room conditions must be maintained during fabrication process especially applicable to lithography process. Any dust particle on silicon wafer can cause defect in the final resist coating. Thus, a clean room facility is necessary for fabrication. Clean room is rated as Class according to the maximum number of particles of 0.5µm diameter per cubic foot of air. Class 100 to Class 1 clean room is now being used for VLSI/ULSI fabrication process. Class 100 shall mean the air filtration system is able to filter all particles of diameter size greater than 0.5µm and filtered air has less than 100 dust particles of diameter size less than 0.5µm per cubic foot of air. Likewise Class 1,000 shall mean the air filtration system is able to filter all particles of diameter size greater than 10.0µm and filtered air has less than 10 dust particles of diameter size less than 10.0µm per cubic foot of air. Figure 2.15 shows the number of particle versus the diameter of particle expectation for different class of cleanliness for fabrication of the VLSI integrated circuit.

![Figure 2.15: The number of particle and diameter of particle for various classes of cleanliness](image)

The fabrication of integrated circuit IC both MOS and bipolar devices involves a numbers of repeated major process steps. The processes can be broadly classified into wafer cleaning process, oxidation process, lithography (imaging, resist-bleaching and resist development), etching, diffusion/ion implantation, chemical vapor deposition CVD (thin film deposition), epitaxy silicon and
polycrystalline process, physical vapor deposition/metal deposition or evaporation/sputtering, thin film such as silicon nitride $\text{Si}_3\text{N}_4$, titanium nitride TiN, Ti-W alloy, titanium silicide TiSi$_2$, tungsten silicide WSi$_2$ processes, and sintering/rapid thermal annealing RTA.

### 2.5.1 Wafer Cleaning

By nature process, there is a layer of native oxide grown on any wafer due to presence of oxygen in atmosphere and also due to presence of contaminants such as wax, resin, greasy film, sodium chloride, copper, and etc. The wafer needs to be cleaned before fabrication.

Hydrofluoric acid is used to remove oxide that formed on surface of silicon wafer. Ammonia hydroxide sulphuric acid, and hydrogen peroxide are typically used to remove organic contaminants, whilst hydrogen peroxide and hydrochloric acid are used to remove metal contaminants. De-ionized DI water is then used as solvent for cleaning or rinsing. The wafer is finally dried in nitrogen environment to prevent oxidation and contamination. The right proportional mixing of the above mentioned solvents are termed as RCA solution that was developed in 1965. The solutions are divided into solution clean 1 and solution clean 3. Figure 3.8 shows the eight cleaning steps for cleaning the wafer to remove inorganic, organic, and native oxide contaminants before actual fabrication process steps begin. The figure also shows the composition of the various solutions and the temperature requirements during cleaning process.

<table>
<thead>
<tr>
<th>Step</th>
<th>Solution</th>
<th>Temperature</th>
<th>Type of Contaminant to be removed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$ (4:1)</td>
<td>120°C</td>
<td>Organic particle</td>
</tr>
<tr>
<td>2</td>
<td>DI water</td>
<td>25°C</td>
<td>Rinse</td>
</tr>
<tr>
<td>3</td>
<td>$\text{NH}_3\text{OH} + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$ (1:1:5)</td>
<td>80°C – 90°C</td>
<td>Organic particle</td>
</tr>
<tr>
<td></td>
<td>RCA clean 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>DI water</td>
<td>25°C</td>
<td>Rinse</td>
</tr>
<tr>
<td>5</td>
<td>$\text{HCl} + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$ (1:1:6)</td>
<td>80°C – 90°C</td>
<td>Inorganic ion</td>
</tr>
<tr>
<td></td>
<td>RCA clean 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>DI water</td>
<td>25°C</td>
<td>Rinse</td>
</tr>
<tr>
<td>7</td>
<td>HF + $\text{H}_2\text{O}$ (1:50)</td>
<td>25°C</td>
<td>Native oxide</td>
</tr>
<tr>
<td>8</td>
<td>DI water</td>
<td>25°C</td>
<td>Rinse</td>
</tr>
</tbody>
</table>

*Figure 2.16: Cleaning step and composition of RCA solution*
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2.5.2 Oxidation Process

Silicon dioxide $\text{SiO}_2$ is a very good dielectric material. Its dielectric constant is 3.9. Silicon dioxide is used mainly for masking where dopant cannot be diffused, passivation, and insulation.

Oxidation is a process of growing a thin layer of amorphous silicon dioxide. The process is also termed as \textit{chemical vapor deposition CVD}. There are several methods to grow oxide named as the dry and wet methods. Thermal oxide is grown using oxygen and silicon yields dry oxide.

$$\text{Si} + \text{O}_2 \rightarrow \text{SiO}_2 \quad (2.16)$$

or wet oxide is grown using steam and silicon.

$$\text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2 \quad (2.17)$$

Anodic oxide is formed in gaseous or liquid medium by electric field induced transportation of mobile ion. This method is also termed as \textit{low pressure chemical vapor deposition LPCVD}.

Other methods are: low temperature ($400^\circ\text{C}$ to $500^\circ\text{C}$) chemical vapor deposition using silane $\text{SiH}_4$ and oxygen $\text{O}_2$ and high temperature ($1,000^\circ\text{C}$) deposition using tetrachlorosilane $\text{SiCl}_4$ with $\text{CO}_2$, $\text{O}_2$, and $\text{H}_2\text{O}$.

$$\text{SiH}_4 + \text{O}_2 \rightarrow \text{SiO}_2 + 2\text{H}_2 \quad (2.18)$$

The oxidation process described above generally forms an oxide film that covers the entire surface of the wafer. The ability to selective oxidize a particular area on surface of silicon is important in high-density bipolar and MOS processes. It is because selective oxidation has to improve the device pack density and more planar final structures. To achieve this, it utilizes the technique called \textit{localized oxidation of silicon LOCOS} process.

There are two types of LOCOS processes, which would result semi-recessed oxide and fully recessed structure. Oxide grown on silicon wafer without pre-etch process that is not protected by silicon nitride $\text{Si}_3\text{N}_4$ is called \textit{semi-recessed structure}. Full recessed oxide is formed by etching the silicon prior to oxidation. This process can yield a very planar surface after silicon nitride removal. The cross section depicting the process sequence of LOCOS for semi-recessed and fully recessed structures are shown in Fig. 2.17.
The analysis of oxidation process shows that the grown oxide thickness $t_{ox}$ can be approximated by the quadratic equation $t_{ox}(t) = \frac{A}{2} \left[ 1 + \frac{4Bt}{A^2} - 1 \right]$, where $A$ and $B$ are coefficient depending on temperature, crystal orientation and gas mixture. The initial phase of oxide growth is linear which is approximately equal to $\frac{B}{A} t$. As time goes on, the process is slower that follows equation $\sqrt{Bt}$.

One silicon atom is used to form one molecule of silicon dioxide $\text{SiO}_2$. Based on the density of silicon $N_{\text{Si}}$ and silicon dioxide $N_{\text{ox}}$, which are $5.0 \times 10^{22} \text{ cm}^{-3}$ and $3.3 \times 10^{22} \text{ cm}^{-3}$ respectively, the recession is 46% meaning every unit thickness of oxide formed required 0.46 unit thickness of silicon.

![Diagram of LOCOS processes](image)

**Figure 2.17:** Cross section depicting the process sequence for obtaining semi-recessed and fully recessed LOCOS

Trench isolation either shallow or deep refilled types are used in advanced MOS and bipolar processes. Shallow trench isolation STI process step is shown in Fig. 2.18.

![Diagram of STI processes](image)

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Deep trench refilled with polysilicon is used to form trench capacitor used in DRAM memory design. It is also used as isolation in SiGe heterojunction HBT technology. The process step of deep trench refilled with polysilicon with combination of LOCOS field oxidation is shown in Fig. 2.19.

The deep trench is formed from reactive ion etching process. This process can create deep trench of high aspect ratio. The surface of trench is passivated with a layer of thermally grown oxide. The rest of process steps should be self explanatory.
Chemical Mechanical polishing CMP process is introduced in early 1990’s and it is now used to achieve high planar topology for deep submicron process. It is used in both bipolar and MOS processes. The conceptual process technique is shown in Fig. 2.20. The wafer is mounted on a rotating pattern. Liquid slurry is continuous dispensed on the surface of polishing pad. A combination of vertical force between wafer and the abrasive pad as well as the chemical action of slurry is used to polish the surface to highly planar state. Polishing process stops when the nitride layer is fully exposed.

![Chemical mechanical polishing technique](image)

**Figure 2.20:** Chemical mechanical polishing technique

### 2.5.3 Silicon Nitride Deposition

Silicon nitride Si$_3$N$_4$ film is used primarily for two purposes namely as a mask against oxidation because diffusion of oxygen through it very slow and as a final passivation layer on integrated circuit because it is a very barrier against contaminants like water and sodium ion. Generally silicon nitride is not directly deposited in contact with silicon due to poor interface properties especially with regard to fixed or interface trapped charges and stress. It is normally deposited on silicon dioxide.

Reactive sputtering of ammonia or nitrogen is the most common way to deposit this type of film.

\[
3\text{SiH}_4 + 4\text{NH}_3 \xrightarrow{-900^\circ\text{C}} \text{Si}_3\text{N}_4 + 12\text{H}_2 \uparrow \quad (2.19)
\]

or

\[
3\text{SiCl}_4 + 4\text{NH}_3 \xrightarrow{550^\circ\text{C}-1200^\circ\text{C}} \text{Si}_3\text{N}_4 + 12\text{HCl} \uparrow \quad (2.20)
\]
To ensure the proper stoichiometry of the film, an excess of ammonia in the ratio as much as 20:1 over the chloride or silane is used. Nitrogen can also be used in place of ammonia.

Silicon nitride used for final passivation film must be deposited at temperature of 450°C because plasma-enhanced chemical vapor deposition PECVD technique is commonly used.

### 2.5.6 Titanium and Titanium-Tungsten Alloy Deposition

Titanium is often used as an under layer for contacts, vias, and interconnects because of its good adhesion to other materials, its ability to reduce native oxides, and its good electrical contacting properties. It is usually deposited by sputtering, either using standard magnetron sputtering or by using collimated or ionized sputtering for good coverage in contact or via bottom.

Titanium-tungsten alloy Ti-W is used as the barrier metals in contact and as under layers and antireflective layers in the interconnects. However, TiN is more commonly used today because of better thin film and barrier properties. Ti-W is deposited using magnetron sputtering usually from a single target.

### 2.5.7 Tungsten Deposition

Tungsten is commonly used as contact or via metal called tungsten plug or in some cases is used as the first-level metal interconnect. It is usually deposited by chemical vapor deposition CVD due to very good filing ability and conformal coverage in hot wall and low pressure system. The temperature of the deposition is ranged from 250°C – 500°C and total pressure in 0.1 – 0.2 torr range.

Tungsten deposition can also be done by either hydrogen or silane following equations.

\[ \text{WF}_6 + 3\text{H}_2 \rightarrow \text{W} + 6\text{HF} \quad (2.21) \]

or

\[ 2\text{WF}_6 + 2\text{SiH}_4 \rightarrow 2\text{W} + 3\text{SiF}_4 + 6\text{H}_2 \quad (2.22) \]
2.5.8 Titanium Silicide and Tungsten Silicide Deposition

Titanium silicide TiS\textsubscript{i} and tungsten silicide WSi\textsubscript{2} are common silicides used today in silicon microelectronics. Other commonly silicides include CoS\textsubscript{i} \textsubscript{2}, MoS\textsubscript{2}, NiS\textsubscript{2}, and platinum silicide PtS\textsubscript{2}. Silicides are used in CMOS technology extensively with the purpose to reduce the sheet resistance of polysilicon and $n^+$ contact region. Silicides are often as part of the contact structure that can be on top of gate, source, and drain or in the contact hole. Silicide can also be used as local interconnects.

Silicide can be formed either by direct deposition of silicide or by deposition metal on top of silicon followed by the reaction between the metal and silicon to form silicide.

Direct deposition method can be done by sputtering from composite target, co-sputtering from two targets of metal and silicon, co-evaporation of the metal, and chemical vapor deposition.

The reaction method is a commonly method used today. The metal such as titanium is deposited by sputtering process on the exposed gate and/or source/drain regions, which are silicon. The wafer is then annealed and silicide is formed. The un-reacted metal is then etched away.

2.5.9 Titanium Nitride Deposition

Titanium nitride TiN is used as barrier layers in contact and as the under layers and antireflective layers in interconnects. They have mostly replaced Ti-W in the application due to better barrier and film qualities. TiN is normally deposited or formed on top of Ti film which has better contact and adhesion properties to the films underneath. TiN is normally deposited reactive sputtering method, which involves sputtering a metal in the presence of a reactive gas such as nitrogen or oxygen to form the metal oxide or nitride. CVD method can be used to deposit TiN film with titanium tetrachloride TiCl\textsubscript{4} and ammonia NH\textsubscript{3} at temperature 400-700\textdegree{}C via reaction.

$$6\text{TiCl}_4 + 8\text{NH}_3 \rightarrow 6\text{TiN} + 24\text{HCl} + \text{N}_2$$ (2.23)

2.5.10 Lithography

Lithography is a process encompasses all the steps involved in transferring a pattern from a mask to the surface of silicon wafer. This is also a process to
create precise dimensioned open area on silicon dioxide/silicon nitride or metallic surface. Opening on silicon dioxide surface will allow diffusion or doping of other impurities. There are two methods to do this. They are optical lithography and electron beam or ion beam lithography.

Before we continue to describe the lithography process steps, let’s discuss the process requirements for achieving lithography process steps. A mask is necessary for transferring the integrated circuit pattern on the silicon. The mask is made by mask making machine that transfer either an electron beam or laser pattern generator. The pattern of IC for each mask is literally written on a mask blank using scanning electron beam or laser beam. The mask is usually made of fused silica plate covered with a thin layer ∼ 80nm of chromium and a layer of photoresist. A thin antireflection coating layer of 10-15nm is also often used between the chrome and the photoresist to prevent reflection from chrome layer which can degrade pattern resolutions. The electron beam or laser is then exposes the photoresist which is then developed and used as an etch mask to transfer the mask pattern into the chrome. The chrome is then wet etch or dry etch when the dimension is getting smaller and removed the photoresist. The fused silica has a high polished surface so that the light is not scattered as it passes through the mask and ideally has a small thermal expansion coefficient so that the mask dimensions are stable over small temperature range.

Another important requirement is the light source. Traditionally the light source is the arc lamps as the primary source. The lamp usually contains mercury vapor inside the sealed glass envelope. Two conducting electrodes inside the envelope are separated by several mm. An arc is struck between the electrodes by applying a high voltage typically several kV to ionize the gas. Once the gas is ionized, it behaves like plasma. In the modern lithography, deep UV light of wavelength either 193nm or 248nm, electron beam, ion beam, X-ray are used as the light source.

The process steps of photolithography are clean wafer, deposit barrier layer of SiO₂, Si₃N₄, metal, coating with photoresist, soft bake, align mask, expose pattern, develop photoresist, hard bake, etch windows in barrier layer, and removal of photoresist. In brief, photolithography has three steps i.e. imaging, resist bleaching, and resist-development.

Before imaging is made, the wafer is coated with a layer of photoresist, an organic compound, which is either light sensitive or non-light sensitive. A mask containing the pattern of the IC design, is used either to block out the required part or non-required part on the wafer. Example of the photoresist is
polyisoprene derivative. There are two types of photoresist. The positive type is light sensitive to ultra violet UV or other light source, acid-resist organic polymer, initially insoluble to developing solution and after exposure becomes soluble to developing solution. The negative photoresist is initially soluble to developing solution, after exposing to UV light becomes insoluble.

Selective exposing the photoresist needs a chrome-coated glass or quartz as mask used to cover the area so that it is opaque. The photoresist is developed in flowing aqueous alkaline or trichloroethylene and then bake in the oven.

2.5.11 Etching

After a thin film layer is deposited on the wafer surface, it is selectively removed by etching to leave the desired pattern of the film on the wafer surface. Several techniques are used to transfer the resist pattern to the silicon wafer. Wet etch and dry etch or plasma etch are the common methods. With decrease feature size with the need of smaller line width and more vertical structure required, dry etching is preferred than wet etching in a few aspects that are discussed in the following texts.

**Wet Etch.** The first etchant used in the integrated circuit industry was simple wet chemical etchant. By immersing the wafer into the bath of liquid chemical, the exposed films could be etched away leaving unetched region of the film that was masked with photoresist or other films.

Silicon dioxide $\text{SiO}_2$ is usually removed by hydrofluoric acid HF or hydrochloric acid HCL, whilst aluminum interconnects can be removed by phosphoric acid.

$$\text{SiO}_2 + 6\text{HF} \rightarrow 2\text{H}_2\text{SiF}_6 + 2\text{H}_2\text{O} \quad (2.24)$$

The by-product $\text{H}_2\text{SiF}_6$ is water soluble complex which can be removed by cleaning.

For the case of etching silicon $\text{Si}$, the common etchant is the mixture of nitric acid $\text{HNO}_3$ and hydrofluoric acid HF. The etching occurs by first oxidizing the surface of the silicon to form silicon dioxide by partially decomposed nitric acid into nitrogen dioxide following equation.

$$\text{Si} + 2\text{NO}_2 + 2\text{H}_2\text{O} \rightarrow 2\text{H} + 2\text{HNO}_2 \quad (2.25)$$
2 Device Fabrication

The hydrofluoric acid then dissolves the silicon dioxide by reaction given in equation (2.24).

The photoresist is removed with sulphuric acid $\text{H}_2\text{SO}_4$ and hydrogen peroxide $\text{H}_2\text{O}_2$ for wafer without metal. For wafer with metal, organic stripper is used.

Wet etch can be very selective because it depends on the chemistry. The limiting steps in most etch process is usually the chemical reaction in which the etch species react with the film forming soluble by-product. The selectivity $S$ of an etch process between two material 1 and 2 is simply the ratio of their etch rate $r$ in the etchant, which follows equation.

$$ S = \frac{r_1}{r_2} \quad (2.26) $$

Material 1 is usually the film being etched and material 2 is either the masking material such as photoresist and silicon dioxide $\text{SiO}_2$ or material below the film.

Dry Etch. Dry etch or plasma etch is based on reactive ion-etch process and plasma-etch. This process is widely used in VLSI fabrication.

They are two major reasons why dry etch is used. In the etching of silicon nitride, the wet etch process is very slow and not selective with respect to silicon dioxide. Moreover, the HF etchant often causes lift off problem to photoresist masking so that $\text{SiO}_2$ mask has to be used.

The dry etch allows directional or anisotropic etching. Directional etching is needed to minimize under etching and etching bias, which allows smaller and more tightly packed structure. The directional etch is due to the presence of ionic species in the plasma and electric field that directs them normal to the wafer surface.

2.5.12 Epitaxial Silicon and Polycrystalline Deposition

Epitaxial silicon is silicon that is deposited on top of single crystal material usually the silicon substrate. The epitaxial silicon atoms arrange themselves following the crystal arrangement of the substrate. If there is no underlying single crystal silicon is present or if the deposition conditions are not right, then amorphous or polycrystalline silicon will be formed.
One of the processes is deposition by chemical vapor deposition process CVD using tetrachloride SiCl$_4$. The silicon tetrachloride reacts with hydrogen to form polycrystalline, which has chemical equation shown below

$$\text{SiCl}_4 + 2\text{H}_2 \xrightarrow{1200^\circ\text{C}} \text{Si} + 4\text{HCL} \quad (2.27)$$

Deposition of epitaxial silicon can be also achieved using LPCVD process using thermal decomposition of silane SiH$_4$ in hydrogen environment.

$$\text{SiH}_4 \xrightarrow{\text{H}_2, \text{atm,phere 600^\circ\text{C}}} \text{Si} + 2\text{H}_2 \uparrow \quad (2.28)$$

Polycrystalline silicon can be deposited on arbitrary substrate and does not require exposed silicon underneath. It is usually used for gate electrode in CMOS technology and for local interconnected resistor.

Polycrystalline silicon is characterized by low resistivity of doped silicon. It is a process of growing another layer of doped silicon crystal on the existing silicon crystal or silicon dioxide. The process involved for making polycrystalline silicon is similar to that of epitaxial silicon growth. Polycrystalline silicon can be deposited using sputtering process.

### 2.5.13 Diffusion

Diffusion of impurities is typically done by placing semiconductor wafers in a carefully controlled, high temperature quartz-tube furnace and passing a gas mixture that contain the desired dopant through it. Thus, its purpose is to introduce dopant into silicon crystal. Mixture of oxygen and dopants such as diborane and phosphine are introduced in the furnace with the exposed wafer surface at temperature ranges between 800$^\circ$C and 1,200$^\circ$C for silicon and 600$^\circ$C and 1,000$^\circ$C for gallium arsenide GaAs. The number of dopant atoms that diffuse into the semiconductor is related to the partial pressure of the dopant impurity in the gas mixture.

Dopant can be introduced by solid source (e.g. BN for boron, As$_2$O$_3$ for arsenic, and P$_2$O$_5$ for phosphorus), gases source (e.g. B$_2$H$_6$, AsH$_3$, and PH$_3$), and liquid source (e.g. BBr$_3$, AsCl$_3$, and POCl$_3$). The chemical reaction for phosphorous diffusion is shown in equation (2.29).

$$4\text{POCl}_3 + 3\text{O}_2 \rightarrow 2\text{P}_2\text{O}_5 + 6\text{Cl}_2 \uparrow \quad (2.29)$$
2 Device Fabrication

The $\text{P}_2\text{O}_5$ forms a glass-on-silicon wafer and then reduced to phosphorous by silicon following equation (2.30).

$$2\text{P}_2\text{O}_5 + 5\text{Si} \rightarrow 4\text{P} + 5\text{SiO}_2 \uparrow \quad (2.30)$$

The phosphorous is released and diffused into silicon and chlorine $\text{Cl}_2$ gas is vented away.

For diffusion in gallium arsenide, the high vapor pressure of arsenic requires special method to prevent loss of arsenic by decomposition or evaporation. These methods include diffusion in sealed ampules with over pressure of arsenic and diffusion in an open-tube furnace with doped oxide capping layer such as silicon nitride. Most of the studies on $p$-type diffusion have been confined to the use of zinc in the forms of $\text{Zn-Ga-As}$ alloys and $\text{ZnAs}_2$ for the sealed-ampule approach or $\text{ZnO-SiO}_2$ for the open-tube approach. The $n$-type dopants in gallium arsenide include selenium and tellurium.

To complete the process, 'drive in' or re-distribution of dopant is done in nitrogen or wet oxygen where silicon dioxide $\text{SiO}_2$ is grown at the same time.

2.5.14 Ion Implantation

Ion implantation has been the dominant doping technique for silicon integrated circuit manufacturing for 30 years. This process is expected to be in the position of dominance for the foreseeable future.

Like diffusion process, it is a process where dopant is introduced using ion species such as $\text{BF}_3$ and $\text{PF}_5$. The ion species are ionized and accelerated to mass separation magnet where they are targeted at the wafer surface. The implantation energies are between 1.0keV and 1.0MeV. It would result an ion distribution with average depths ranging from 10nm to 10µm. Ion doses vary from $10^{12}$ ions/cm² for threshold voltage adjustment to $10^{18}$ ions/cm² for formation of buried insulating layer. The main advantage over the diffusion is low temperature, more precise control and reproducibility of impurity doping, and shallow implant. However, due to high-energy bombardment, Rapid thermal annealing RTA at 400°C to 500°C is required to allow the implanted atom to stay at the right substitutional site and at the same time to repair crystal damage.
2.5.15 Metallization

Aluminum is the main interconnect material in silicon microelectronics. Pure aluminum is usually not used but an alloy of aluminum Al with 0.5-1.0 wt. percent Cu to prevent hillock and electromigration and sometimes with about 1.0 wt. percent silicon to prevent spiking and other interaction.

The most common methods of physical vapor deposition PVD of metals are evaporation, e-beam evaporation, plasma spray deposition, and sputtering. Aluminum film can be deposited by PVD or CVD. Since aluminum and its alloys have low resistivity, these metals satisfy the low resistivity from 3.7$\mu\Omega$-cm for Al to 3.5$\mu\Omega$-cm for its alloys requirements. Aluminum also adheres well to silicon dioxide.

Aluminum deposition can be done on high temperature reactive sputtering using electrical discharge at 1,000 to 3,000V. This is a process of chemical vapor deposition. It can also be done in vacuum vapor deposition by heating tungsten filament or electron beam evaporation in vacuum. Other methods used are filament evaporation, electron-beam evaporation, flash evaporation etc.

2.5.16 Molecular Beam Epitaxy

Molecular beam epitaxy MBE and chemical vapor deposition CVD are advanced methods used to growth thin film. Between these two methods, MBE is an ultra high vacuum UHV method with base pressure at about Torr, whereas CVD method is a low-vacuum technique with based pressure about Torr or greater). A CVD method for growing epitaxial layers by employing metal-organic gases is referred to as metal-organic chemical vapor deposition MOCVD. These epitaxial techniques are commonly employed for the formation of various structures with desired properties in energy band-gap engineering, such as superlattices and quantum wells QWs

A schematic illustration of an MBE system is shown in Fig. 6.2.
In this UHV MBE technique, several source cells, which are referred as effusion cells supply fluxes of molecular beams of various species that impinge upon a heated substrate such as at temperature 580°C in the case of GaAs. Each separate effusion cell, which is used for individual constituents of required material, is equipped with a shutter that allows emission and termination. The slow growth rates of less than 1.0nm/s allow growing high-quality crystalline materials, and opening or closing shutters allows controlling the film stoichiometry (reactant and product relationship in chemical reaction) and doping levels within a mono layer. MBE technique used for growing epitaxial layers allows possibility to construct artificial structures in which layers of different materials and thickness alternate structures to be fabricated. The period of the layers may be as small as a few mono layers.

The main advantages of MBE technique include its suitability for mono layer growth with atomically abrupt interfaces and great uniformity, stoichiometry and impurity control. Reflection high-energy electron diffraction RHEED can be employed as an in situ monitoring tool in MBE. In this method, high-energy electrons in the range between about 5 and 50keV, striking the sample at a grazing angle between about 1 and 5° are scattered by the first few atomic layers of sample surface. The pattern produced on a phosphor screen positioned opposite the electron gun can be monitored. From the features of such RHEED patterns (i.e., from the spacing and symmetry of the features and from intensity oscillations), information such as the surface structure and...
coverage, as well as on the degree of surface roughness and film growth mechanism can be derived. Thus, this method (i.e., the time evolution of the RHEED pattern during epitaxy) allows monitoring of structural changes in the film during its growth or during its post-growth annealing.

2.5.17 Sintering/Annealing

Sintering is done in nitrogen environment to establish intimate contact between silicon and aluminum. Rapid thermal annealing RTA is a process using to repair damage due to implantation and move the implanted ion to right substitutional site. The process is also used to drive-in the impurity.

2.6 Fabrication of Bipolar Junction Transistor

Traditionally bipolar junction transistor is mostly fabricated using junction isolation process. However, nowadays oxide isolation, dielectric isolation, self aligned double polysilicon process etc are commonly used to fabricate advanced bipolar junction transistor. The flowchart of the process steps involving seven mask sets are shown in Fig. 2.22.

Figure 2.22: The fabrication process steps of junction isolation bipolar junction transistor
2 Device Fabrication

An pictorial illustration of the processes for fabricating two *nnp* bipolar junction transistor are shown in Fig. 2.23. The transistors are built with a *p*-type substrate.

The *p*⁺ is used as the isolation, which is called *junction isolation* and the *p* substrate is tied to the most negative voltage of the circuit. It is usually tied to *V)]; which is ground most of the time. This creates the reverse biasing of the *p*⁺ and *n* epitaxial layer junction that forms a natural isolation.

![Figure 2.23: Step by step fabrication of *nnp* bipolar transistor](image-url)
Figure 2.23(a) shows the wafer type for the fabrication of bipolar junction transistor is a $p$-doped (111) orientation type. Figure 2.23(b) illustrates the devices after finishing fabricating the $n^+$ deep diffused barrier layer. Figure 2.23(c) illustrates the formation of polycrystalline and silicon dioxide step. Figure 2.23(d) illustrates the formation of $p^+$ junction isolation. Figure 2.23(e) shows the top view of devices shown Fig. 2.22(d) after the removal of silicon dioxide. Figure 2.23(f) shows the formation $p$-base material for the transistors. Figure 2.23(g) shows the top view of devices shown in Fig. 2.23(f). Figure 2.23(h) shows the formation of $n^+$ emitter and $n^+$ contact diffusion for collector. Figure 2.23(i) shows the side view of the bipolar junction transistor with the aluminum interconnect put in-placed. From Fig. 2.23(i), the two $n$p$n$ bipolar junction transistors are connected as a current mirror circuit. Figure 2.23(j) shows the top view of devices shown in Fig. 2.23(i).

### 2.7 Fabrication of CMOS Transistor

There are many process steps for fabrication of CMOS transistors. Listed here is a 41-step SAJI processes which are shown in Fig. 2.24. In this section, the process steps mentioned in the figure are not fully covered sequentially.

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<td>39</td>
<td>Deposition of $Si_3N_4$</td>
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**Figure 2.24:** CMOS process steps

The fabrication of $n$-MOS and $p$-MOS transistors in a $p$-type (100) wafer that normally has about 300 to 600µm thickness and resistivity 5.0-50.0Ω-cm, is shown in this section. $N$-region must be introduced to accommodate the process
of p-MOS and it is called an *n-well process*. The first process of the fabrication involves growth a thin layer thermal oxide. It is then followed creating an *n*-well region using mask #1 by etching away the oxide. The similar mask is used to dope the *n*-well by the process of ion implantation. After ion implantation, the wafer is annealed to repair crystal damage as the result of ion implantation process. Finally the oxide is stripped. Figure 2.25 and 2.26 illustrate the process of *n*-well formation.

![Diagram](image1)

**Figure 2.25: n-well implant**

![Diagram](image2)

**Figure 2.26: n-well**

Active area such as gate, drain and source and field oxide FOX formations are the next process step utilizing mask #2. As it is illustrated in Fig. 2.27, thermal oxide is growth first and silicon nitride Si$_3$N$_4$ is next step. The mask #2 used to define the field oxide FOX region as the isolation is shown in Fig. 2.28. At this point of process, ion implantation is also used to adjust the threshold voltage of the *n*-MOS and *p*-MOS transistors.
Polysilicon gate is a next step utilizing mask #3. As it is illustrated in Fig. 2.29, the thin layer of thermal oxide is grown before the polysilicon layer. The mask #3 is then used to mask out unwanted polysilicon to create the gate of the $n$-MOS and $p$-MOS transistors as illustrated in Fig. 2.30.
2 Device Fabrication

Mask #4 and #5 are alternatively used to create lightly doped drain LDD aimed to reduce short channel effect due to hot electrons and hot holes phenomena. Figure 2.31 illustrates the lightly doped drain LDD process for \( p \)-MOS transistor, whilst Fig. 2.32 illustrates the lightly doped drain LDD process for \( n \)-MOS transistor. Note that the photoresist will block implant ion but the ion implant can penetrate the oxide layer.

Figure 2.31: LDD implant of \( p \)-MOS transistor

Figure 2.32: LDD implant of \( n \)-MOS transistor
The next process is spacer formation, which is simply growing oxide to cover the polysilicon gate using LPCVD with silane SiH$_4$ and oxygen at 400°C. It is then followed by anisotropic plasma etching to form the spacer. The processes are illustrated in Fig. 2.33 and 2.34 respectively. This process step is preparing for creating a self-aligned heavily doped drain and source for the $n$-MOS and $p$-MOS transistors.

Upon finishing the creation of spacer, the next step is deep $p^+$ and $n^+$ implant which are illustrated in Fig. 2.35 and Fig. 2.36 respectively. It is done by removing the old photoresist and lithography process and etching and boron implant for $p$-MOS transistor and arsenic implant for $n$-MOS transistor.
The photoresist is used to block the unwanted ion implant to the silicon surface. It is used alternatively to block boron during the implant to penetrate to source and drain of the $n$-MOS transistor. During the arsenic implant, it is used to block arsenic from penetrating to source and drain of $p$-MOS transistor.

The next process step is the sputtering process whereby a thin film layer of titanium approximately 50-100nm is deposited as shown in Fig. 2.37. Titanium atom is physically knocked off by bombarding titanium, with argon ion $\text{Ar}^+$. 
The next process steps are heating the wafer in nitrogen environment at about 600-700°C for about a minute. At this temperature, titanium reacts with silicon to form titanium silicide TiSi$_2$ (red color) providing good contact for drain and source and poly gates. Nitrogen also reacts with titanium to form titanium nitride TiN (brown color), which is used as conductor for short-distance local interconnect. The illustration for the titanium silicide and silicon nitride layers is shown in Fig. 2.38.

The next process step is a step selectively to remove the unwanted titanium nitride TiN. It is done by applying photoresist and mask #6. The exposed TiN is then etched away in NH$_4$OH:H$_2$O$_2$:H$_2$O (1:1:5) solution. The defined titanium nitride to be retained after etching is shown in Fig. 2.39.
The followed by process step is to remove photoresist and heat the wafer in argon Ar environment to further reduce the resistivity of titanium nitride TiN and TiSi$_2$. Oxidation and CMP processes are the next two process steps. The device after finished process steps is shown in Fig. 2.40.

Mask #7 is used to provide metal contact as illustrated in Fig. 2.41 and Fig. 2.42 respectively. The process is done by growing silicon diode and lithography to etch the oxide that will provide contact with drain and source of the transistors. The cut in oxide is then filled with metal to get the via. The via is used to connect the drain and source of the MOS transistors to metal 1 level just like the pillars of the bridge or road connected to the foundation and the surface of the road.
After process step shown in Fig. 2.41, titanium nitride TiN (brown color) is deposited by sputtering process. The titanium nitride is used to provide good adhesion to the silicon dioxide SiO$_2$. The following step is depositing a blanket of tungsten W by CVD process. CMP process is the next step for planarization. The final step is the aluminum sputtering process as shown in Fig. 2.42.

The rest of processes are mainly the metal process, which are illustrated in Fig. 2.43 through Fig. 2.45. Figure 2.44 illustrates the device after adding the silicon dioxide that isolates the metal interconnect. Owing to the complexity of the circuit, which is dependent on the number transistor, the number of metal level can be varied from two layers to eight to nine layers for the case of microprocessor device. As illustrated in Fig. 2.45, the device has three metal layers not including the final metal layer for bond pad.
The final layer is the passivation layer, whereby the surface top of the integrated circuit is covered with a layer of glass with selective opening for providing bond pad for wire connection to the device’s package. The illustration of the passivation layer with access cut for bonding is shown in Fig. 2.46.
**Figure 2.45:** High level metal layers and vias

**Figure 2.46:** Top metal and passivation layer
2 Device Fabrication

2.8 Pictorial View of Wafer Preparation and Wafer Fabrication

Pictorial view of some process steps for wafer preparation and wafer fabrication are shown in figures below. The pictures shown here are some examples.

Figure 2.47: Silicon ingot
Figure 2.48: Cleaning room attire

Figure 2.49: Wafer mask and 10X reticle
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Figure 2.50: Cleaning station

Figure 2.51: Epitaxial furnace
Figure 2.52: Lithography - pattern generator

Figure 2.53: Lithography - step and repeat machine
Figure 2.54: Diffusion furnace

Figure 2.55: Ion implanter
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Figure 2.56: Etch station

Figure 2.57: Wafer with fabricated integrated circuit
Figure 2.58: Chemical-mechanical polishing machine
Exercises

2.1. Silicon has diamond crystal structure, the lattice constant $5.43 \, \text{Å}$, and the atomic weight is $28.09 \text{g}$. Show that the density of silicon is $2.33 \, \text{gcm}^{-3}$.

2.2. Gallium arsenide GaAs has zinc blende crystal structure, the lattice constant $5.65 \, \text{Å}$, and the atomic weight is $144.63 \text{g}$. Show that the density of GaAs is $5.32 \, \text{gcm}^{-3}$.

2.3. $\text{Al}_x\text{Ga}_{1-x}\text{As}$ has zinc blende crystal structure and its density is $(5.36 - 1.6x) \, \text{gcm}^{-3}$. Given that atomic weight of Al, Ga, and As are $26.98$, $69.72$, and $74.92 \text{g}$ respectively.
   
   i. Calculate the lattice constant for $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$.
   
   ii. Calculate the surface density of the $(0,0,1)$ plane.
   
   iii. Calculate the surface density of the $(0,1,1)$ plane.

2.4. Determine the number of indium atom per $\text{cm}^2$ on the $(1,0,0)$ surface of an InAs wafer. The lattice constant of InAs is $6.04 \, \text{Å}$.

2.5. Tetrahedral is the primitive cell of silicon crystal structure. Its lattice constant is $5.43 \, \text{Å}$. Calculate the distance between two nearest silicon atoms.

2.6. Given a unit cell is filled with identical hard spherical atom in diamond lattice, calculate the maximum fraction of unit cell volume.

2.7. Determine the Miller indices of the shaded plane in the figure.
2.8. Tetrahedral is the primitive cell of silicon crystal structure. Its lattice constant is $5.43 \, \text{Å}$. Calculate the distance between two nearest silicon atoms.

2.9. Tetrahedral is the primitive cell of silicon crystal structure. Its lattice constant is $5.43 \, \text{Å}$. Calculate the adjacent angle between two covalent bonds of the silicon atoms.
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2.10. Given a silicon wafer to you, how do you identify its crystal orientation and the type of dopant it contains?

2.11. A silicon ingot contains $10^{16}$ boron atoms cm$^{-3}$ is to be grown by the Czochraski technique. What is the concentration of born atoms should be in the molten silicon to give the required concentration in ingot? If the initial load of silicon in crucible is 60kg, how many gram of boron (atom weight is 10.8g) should be added? The density of molten silicon is given to be 2.53gcm$^{-3}$.

2.12. State the reason for necessity to have the titanium silicide and tungsten silicide deposition.

2.13. What is the purpose of titanium nitride deposition?

2.14. Describe the purpose of photolithography.

2.15. List the steps involved in fabrication of a monolithic IC.

2.16. Explain how isolation between components is obtained in an IC.

2.17. Sketch the cross section of $nnp$ bipolar junction transistor.

2.18. Criticize missing step and re-draw the flowchart mentioned in Fig. 2.22 to reflect the actual process steps for fabrication of an $nnp$ bipolar junction transistor.
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