Chapter 4

Semiconductor Materials

Alternative Device Structures
<table>
<thead>
<tr>
<th>Chapter 4 Alternative Device Structures</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.0 Introduction</td>
<td>147</td>
</tr>
<tr>
<td>4.1 Basic MESFET Operation</td>
<td>148</td>
</tr>
<tr>
<td>4.2 Basic MESFET Technology</td>
<td>149</td>
</tr>
<tr>
<td>4.3 Modulation Doping Field Effect Transistor</td>
<td>150</td>
</tr>
<tr>
<td>4.3.1 Analysis of Current Equations</td>
<td>154</td>
</tr>
<tr>
<td>4.4 mHEMT and pHEMT Devices</td>
<td>156</td>
</tr>
<tr>
<td>4.5 Monolithic Microwave Integrated Circuit MMICs</td>
<td>161</td>
</tr>
<tr>
<td>4.6 Optoelectronic Devices</td>
<td>165</td>
</tr>
<tr>
<td>4.7 Heterojunction Bipolar Junction Transistor</td>
<td>170</td>
</tr>
<tr>
<td>Exercises</td>
<td>173</td>
</tr>
<tr>
<td>Bibliography</td>
<td>174</td>
</tr>
<tr>
<td>Figure 4.1:</td>
<td>3-D structure of a simple mesa-isolated MESFET</td>
</tr>
<tr>
<td>Figure 4.2:</td>
<td>Process flow of a simple mesa-isolated MESFET</td>
</tr>
<tr>
<td>Figure 4.3:</td>
<td>Energy band diagram of $n^+$-Al$<em>{0.3}$Ga$</em>{0.7}$As/$n$-GaAs heterojunction</td>
</tr>
<tr>
<td>Figure 4.4:</td>
<td>A schematic of a recess-gate $n^+$-Al$<em>x$Ga$</em>{1-x}$As/GaAs MODFET</td>
</tr>
<tr>
<td>Figure 4.5:</td>
<td>Energy band diagram of $n^+$-Al$<em>x$Ga$</em>{1-x}$As and GaAs MODFET at thermal equilibrium</td>
</tr>
<tr>
<td>Figure 4.6:</td>
<td>Energy band diagram of $n^+$-Al$<em>x$Ga$</em>{1-x}$As and GaAs MODFET for $V_G &gt; V_t$</td>
</tr>
<tr>
<td>Figure 4.7:</td>
<td>Types of MODFET structures (a) conventional unstrained MODFET on GaAs and InP substrates, (b) pseudomorphic MODFET, and (c) metamorphic MODFET</td>
</tr>
<tr>
<td>Figure 4.8:</td>
<td>Two types of the most common AlGaN/GaN HFET structures</td>
</tr>
<tr>
<td>Figure 4.9:</td>
<td>(a) AlGaN/GaN with source, drain and gate directly deposited on surface of AIGN (b) AlGaN/GaN with additional oxide layer</td>
</tr>
<tr>
<td>Figure 4.10:</td>
<td>Top view of a typical AlGaN/GaN HFET</td>
</tr>
<tr>
<td>Figure 4.11:</td>
<td>A single heterojunction AlGaN/GaN HFET and its conduction band diagram</td>
</tr>
<tr>
<td>Figure 4.12:</td>
<td>A double heterojunction AlGaN/GaN HFET and its conduction band diagram</td>
</tr>
<tr>
<td>Figure 4.13:</td>
<td>A two channel heterojunction AlGaN/GaN HFET and its conduction band diagram</td>
</tr>
<tr>
<td>Figure 4.14:</td>
<td>Cross sectional of a typical MMIC</td>
</tr>
<tr>
<td>Figure 4.15:</td>
<td>Interdigitated and sample overlay capacitor</td>
</tr>
<tr>
<td>Figure 4.16:</td>
<td>Air bridge process steps for forming spiral inductor</td>
</tr>
<tr>
<td>Figure 4.17:</td>
<td>(a) Coplanar interconnect and (b) microstrip interconnect</td>
</tr>
<tr>
<td>Figure 4.18:</td>
<td>Injection of minority carrier and subsequent radiative recombination with majority carrier in a forward bias $pn$ junction</td>
</tr>
<tr>
<td>Figure 4.19:</td>
<td>Semiconductor laser structure in Fabry-Perot cavity configuration (a) Homojunction laser, (b) double-heterojunction laser DH, and (c) stripe-geometry double-heterojunction laser</td>
</tr>
<tr>
<td>Figure 4.20:</td>
<td>The quantum-well laser</td>
</tr>
<tr>
<td>Figure 4.21:</td>
<td>GaInAs/GaInAsP multiple-quantum well laser structure</td>
</tr>
<tr>
<td>Figure 4.22:</td>
<td>Emitter-base energy band diagram of homojunction and heterojunction bipolar junction transistor</td>
</tr>
<tr>
<td>Figure 4.23:</td>
<td>An Al$<em>x$Ga$</em>{1-x}$As/ GaAs/ Al$<em>x$Ga$</em>{1-x}$As heterojunction bipolar junction transistor</td>
</tr>
<tr>
<td>Figure 4.24:</td>
<td>A Si/SiGe/Si heterojunction transistor</td>
</tr>
</tbody>
</table>
4.0 Introduction

Gallium arsenide GaAs is distinct from silicon in several ways. First it is made in the form of very-high resistivity semi-insulating substrate. This provides a unique advantage for high speed analog application such as amplifiers and receivers for communication and radar. This feature is also made GaAs very useful for building digital integrated circuit that might be exposed to radiation such as that found on satellites. GaAs has high low electric field mobility, which is 8,500cm²/V-s for electron and material is amenable to growth of heterostructures. Both of these characteristics favor for the fabrication of high speed, although the defect density and power dissipation limit the pack density as compared with CMOS devices. Gallium arsenic GaAs and other III-V semiconductors are direct semiconductors. This means that electron-hole recombination is lightly to give up a photon without involvement of momentum. Therefore, GaAs is a popular material for making various light emitting structures like infrared light-emitting diode, laser diode, and solar cell. GaAs is also used to fabricate monolithic microwave integrated circuit MMICs.

Gallium arsenide can be prepared with a number of industrial processes. The crystal growth can prepared using horizontal zone furnace, which is \textit{Bridgeman-Stockbarger technique}, where gallium and arsenic vapor react and deposit on a seed crystal at the cooler end of the furnace. \textit{Liquid encapsulated Czochralski} LEC is another method.

Some techniques used to produce GaAs film are vapor phase epitaxy VPE and metal organic chemical vapor deposition MOCVD. In VPE process, gaseous gallium reacts with arsenic trichloride to form GaAs thin film and chlorine. The equation of chemical reaction is shown in equation (4.1).

$$2\text{Ga} + 2\text{AsCl}_3 \rightarrow 2\text{GaAs} + 3\text{Cl}_2$$  \hspace{1cm} (4.1)

In MOCVD process, tri-methylgallium reacts with arsine to form the GaAs thin film. The equation of chemical reaction is shown in equation (4.2).

$$\text{Ga(CH}_3\text{)}_3 + \text{AsH}_3 \rightarrow \text{GaAs} + 3\text{CH}_4$$  \hspace{1cm} (4.2)
04 Alternative Device Structures

4.1 Basic MESFET Operation

The 3-D structure of a typical mesa isolated gallium arsenic GaAs metal semiconductor field effect transistor MESFET is shown in Fig. 4.1. The internal pinch off voltage $V_p$ is equal to $(V_{bi} - V_G)$, which is also called *intrinsic pinch off voltage*. It is defined as

$$V_p = \frac{qN_Dh^2}{2\varepsilon_S} \tag{4.3}$$

where $h$ is the thickness of the channel. The gate voltage $V_G$ required to cause pinch off is denoted by threshold voltage $V_t$, which is when gate voltage $V_G$ is equal to $V_t$, i.e., $V_t = (V_{bi} - V_p)$. If $V_{bi} > V_p$, then the $n$-channel is already depleted. It requires a positive gate voltage to enhance the channel. If $V_{bi} < V_p$, then the $n$-channel requires a negative gate voltage to deplete.

The gate voltage $V_G$ needed for pinch off for the $n$-channel MESFET device is

$$V_t = V_{bi} - V_p = \phi_b - \frac{kT}{q} \ln \left( \frac{N_C}{N_D} \right) - \frac{qN_Dh^2}{2\varepsilon_S} \tag{4.4}$$

where $\phi_b$ is Schottky barrier potential, which is defined as $\phi_b = \phi_m - \chi_s$. $\phi_m$ and $\chi_s$ are metal work function and electron affinity of semiconductor. $N_C$ is the effective density of state in conductor band of the semiconductor respectively. For GaAs semiconductor, the value of $N_C$ is $4.7 \times 10^{17}$ cm$^{-3}$.

![Figure 4.1: 3-D structure of a simple mesa-isolated MESFET](image-url)
Like the MOSFET device, the current characteristics of the MESFET have the linear and saturation values, which are governed by the equation (4.5) and (4.6) respectively.

\[
I_D = \frac{q\mu_n N_D Wh}{L} \left\{ V_D - \frac{2\left( (V_D + V_{bi} - V_G) \right)^{3/2} - \left( V_{bi} - V_G \right)^{3/2}}{3(qN_D h^*/2\varepsilon)^{3/2}} \right\} \tag{4.5}
\]

for \(0 \leq V_D \leq V_{Dsat}\) and \(V_P \leq V_G \leq 0\).

\[
I_{Dsat} = g_o \left\{ \frac{V_P}{3} - V_{bi} + V_G + \frac{2\left( V_{bi} - V_G \right)^{3/2}}{3V_P^{1/2}} \right\} \tag{4.6}
\]

for \(V_D \geq V_{Dsat}\) and \(V_G \leq V_P\). \(g_o\) is the channel conductance, which is defined as \(g_o = \frac{q\mu_n N_D Wh}{L}\).

4.2 Basic MESFET Technology

Wide variety of GaAs MESFET technologies has been developed. The basic depletion-mode technology is shown here. It requires three to five masks. Figure 4.2 shows the process flow for a simple mesa-isolated MESFET.

**Figure 4.2:** Process flow of a simple mesa-isolated MESFET
04 Alternative Device Structures

A semi-insulating substrate is first coated with a thin layer of silicon nitride Si$_3$N$_4$ for preventing contamination and then implanted with silicon to form the active conducting channel as shown in Fig. 4.2(a). The silicon implant should be in the region 1 to 6.0x10$^{17}$ cm$^{-3}$. Alternatively this step can be replaced by forming a epixial layer. This can be done either by MOCVD or MBE techniques.

The diffused ohmic contact formation step is shown in Fig. 4.2(b). The diffused contact is formed by evaporating a Ni/AuGe sandwich using liftoff method and sintering the contact at about 450$^\circ$C. The drain-to-source separation is usually 3 to 4µm.

After the ohmic contact step, the gate recess and mesa are isolated by wet chemically etching the field region through the active layer to the semi-insulating substrate as shown in Fig.4.2(c) and Fig. 4.2(d). At this point, the pinch-off voltage characteristic is measured using mercury probe or the drain-to-source ungated current-voltage characteristic is measured directly. If the pinch-off voltage needs to be adjusted then it is done by recessing the channel to the desired value. The common etchant for GaAs includes various proportion of sulphuric acid H$_2$SO$_4$, hydrogen peroxide H$_2$O$_2$, and water H$_2$O. For maximum repeatability, a slow etch is required.

The schottky gate electrode is then deposited to form a moderately doped GaAs. Metal must be adhered to GaAs. The commonly chosen metals are titanium/platinum/gold Ti/Pt/Au and titanium/palladium/gold Ti/Pd/Au.

4.3 Modulation Doping Field Effect Transistor

In order to maintain high transconductance for MESFET devices, the channel conductance must be as high as possible, which can be seen from equation (4.5) and (4.6) for MESFET device. The channel conductance is dependent on the mobility and doping concentration. But increasing doping concentration would lead to degradation of mobility due to scattering effect from ionized dopant. Thus, the ingredient is to keep concentration low and at the same time maintaining high conductivity. As the result of this need, heterojunction modulated doping field effect transistor MODFET is the choice.

The most-common heterojunctions for the MODFETs are formed from AlGaAs/GaAs, AlGaAs/InGaAs, InAlAs/InGaAs, and Al$_x$Ga$_{1-x}$N/GaN heterojunctions. The better MODFET is fabricated with MBE or MOCVD etc and it is an epitaxially grown heterojunction structures.
Al$_x$Ga$_{1-x}$As/GaAs MODFET is an unstrained type of heterojunction. This is because the lattice constants of GaAs (5.65 Å) and AlAs (5.66 Å) are almost the same except the energy band-gap. The energy band-gap of GaAs is 1.42eV, while the energy band-gap of AlAs is 2.16eV. The energy band-gap of the alloy can be calculated using equation $E_G^{\text{Alloy}} = a + bx + cx^2$, where $a$, $b$, and $c$ are constant for a particular type of alloy. For Al$_x$Ga$_{1-x}$As, $a$ is equal to 1.424, $b$ is equal to 1.247, and $c$ is equal to 0.

For MODFET fabricated with Al$_x$Ga$_{1-x}$As/GaAs material, the approach is to create a thin undoped well such as GaAs bounded by wider band-gap modulated doped barrier AlGaAs. The purpose is to suppress impurity scattering. When electrons from doped AlGaAs barrier fall into the GaAs, they become trapped electrons. Since the donors are in AlGaAs layer not in intrinsic GaAs layer, there is no impurity scattering in the well. At low temperature the photon scattering due to lattice is much reduced, the mobility is drastically increased. The electron is well below the donor level of the wide band-gap material. Thus, there is no freeze out problem. This approach is called modulation doping. If a MESFET is constructed with the channel along the GaAs well, the advantage would be reduced scattering, high mobility, and no freeze out problem. Thus, high carrier density can be maintained at low temperature and of course low noise. These features are especially good for deep space reception. This device is called modulation doped field effect transistor MODFET and also called high electron mobility transistor HEMT or selective doped HT. Figure 4.3 illustrates the energy band diagram of $n^+$-Al$_x$Ga$_{1-x}$As and $n$-GaAs heterojunction showing $\Delta E_C$ and $\Delta E_G$. The delta energy band-gap between the wide band-gap and narrow band-gap device are determined from equation (4.7) and (4.8) respectively.

$$\Delta E_C = q(\chi_{\text{narrow}} - \chi_{\text{wide}})$$  \hspace{1cm} (4.7)$$

and

$$\Delta E_V = \Delta E_G - \Delta E_C$$  \hspace{1cm} (4.8)$$

$\chi_{\text{wide}}$ and $\chi_{\text{narrow}}$ are respectively the electron affinity of wide band-gap and narrow band-gap semiconductor respectively.
The construction of a recess-gate AlGaAs/GaAs MODFET is shown in Fig. 4.4. The dotted line shows the quantum well where two-dimensional electron gas 2-DEG flows. The undoped AlGaAs, which acts as buffer is 30 – 60 Å thick. The $n$-AlGaAs is around 300 Å thick with concentration of approximately $2 \times 10^{18}$ cm$^{-3}$. For recess-gate type, its thickness is about 500 Å. The source and drain contacts are made of alloy containing Ge such as AuGe. The gate materials can be from Ti, Mo, WSi, W and Al.

Figure 4.5 shows the energy band diagram of the $n^+$-Al$_x$Ga$_{1-x}$As and undoped GaAs under thermal equilibrium, where $\phi_b$ is the Schottky barrier potential.
Figure 4.5: Energy band diagram of $n^+\text{Al}_x\text{Ga}_{1-x}\text{As}$ and GaAs MODFET at thermal equilibrium.

Figure 4.6 shows the energy band diagram of the $n^+\text{Al}_x\text{Ga}_{1-x}\text{As}$ and undoped GaAs under applied gate voltage $V_G$ greater than threshold voltage $V_t$, which shows the 2-dimensional electron-gas 2-DEG. The threshold voltage $V_t$ is defined as the gate voltage $V_G$ applied to the gate such that the Fermi energy level is touching the bottom of the GaAs conduction band.

Figure 4.6: Energy band diagram of $n^+\text{Al}_x\text{Ga}_{1-x}\text{As}$ and GaAs MODFET for $V_G > V_t$. 

- 153 -
04 Alternative Device Structures

In this condition is charge density $n_s$ is at maximum value and the gate has no control on the channel.

An applied negative voltage at gate will begin to deplete the 2DEG in the triangular quantum well. In this condition, the condition band of $n^+$-AlGaAs is moving away from Fermi energy level. The triangular quantum well begins to flatten. Further application of negative gate voltage will eventually completely deplete the 2DEG. This voltage is the threshold voltage $V_t$ and in this condition, the triangular quantum well disappears and the carrier density equals to zero.

4.3.1 Analysis of Current Equations

Using the same approach as the way how to analyze MESFET, the threshold voltage $V_t$ of MODFET is equal to

$$V_t = \phi_b - \frac{\Delta E_s}{q} - V_p$$  \hspace{1cm} (4.9)

$V_p$ is the pinch off voltage, which is potential difference between the modulated donor layer edges as shown in Fig. 4.5. It follows equation (4.10), where $d$ is the barrier thickness and $d_s = d_{ud}$ is the spacer layer thickness and $d_{dop}$ is the thickness of doped layer which is equal to ($d - d_s$).

$$V_p = \frac{q}{\varepsilon_b} \int_0^d N_D(x) dx = \frac{qN_D}{2\varepsilon_b} [d - d_s]^2 = \frac{qN_D}{2\varepsilon_b} d_{dop}^2$$ \hspace{1cm} (4.10)

The space or sheet charge density $n_s$ of the 2-DEG gas at the interface is defined as

$$n_s = \varepsilon_b \frac{\varepsilon_b}{q(d_{dop} + d_{ad} + \Delta d)} [V_G - V_t]$$ \hspace{1cm} (4.11)

where $\Delta d$ is the thickness of mobile electron, which can be approximated as equals to 80 Å. The mobile electron density is equal to zero if the gate voltage $V_G$ is equal to threshold voltage $V_t$.

If gradual channel approximation is applied, the electron or sheet charge distribution $n_s$ across the channel is
\[ n_s(y) = \frac{\epsilon_b}{q(d_{dop} + d_{ud} + \Delta d)} [V_G - V_s - V(y)] \]  

(4.12)

where V(y) is the potential across the channel at distance y from source with drain-to-source bias voltage V_D and source to drain channel length L. The capacitance of n-Al_xGa_{1-x}As is equal to

\[ C_{Al_xGa_{1-x}As} = \frac{\epsilon_b}{d_{dop} + d_{ud} + \Delta d}. \]

Since drift current is the major current component and diffusion current is assumed to be negligible, the current in the channel I_D shall be

\[ I_D = W\mu_q n_s \frac{dV(y)}{dy} \]  

(4.13)

Solving equation (4.13) for boundary conditions y = 0 to y = L for V(y) = 0 to V(y) = V_{DS}, it would yield equation (4.14).

\[ I_D = \frac{W\mu_q n_s \epsilon_b}{(d_{dop} + d_{ud} + \Delta d)L} \left[ V_G - V_s - \frac{V_{DS}}{2} \right] V_{DS}. \]  

(4.14)

At saturation, the drain to source voltage V_{DS} shall be V_{DSSAT} = (V_G - V_t). The saturation current I_{DSSAT} shall follow equation (4.15), which is

\[ I_{DSSAT} = \frac{W\mu_q n_s \epsilon_b}{2(d_{dop} + d_{ud} + \Delta d)L} \left[ V_G - V_s \right]^2 \]  

(4.15)

Since MODFET is a high mobility device, it needs a low critical electrical field \( E_{crit} \) to attain saturation velocity \( v_{sat} \). Thus, the saturation drain-to-source voltage \( V_{DSSAT} \) is \( V_{DSSAT} = E_{crit} L \). The saturation current \( I_{DSSAT} \) at velocity-saturation shall be

\[ I_{DSSAT} = qn_s v_{sat} W \]  

(4.16)

This shall mean that saturation current is independent of channel length L. The transconductance \( g_{mSAT} \) shall be equal to equation (4.17) by differentiating \( I_{DSSAT} \) with respect to gate voltage \( V_G \).

\[ g_{mSAT} = \frac{W\mu_q n_s \epsilon_b}{(d_{dop} + d_{ud} + \Delta d)L} [V_G - V_s] \]  

(4.17)
The cut-off frequency $f_T$ for MODFET shall be

$$f_T = \frac{g_{msat}}{2\pi(WL)_{AlGaAs} + C_{par}}$$  \hspace{1cm} (4.18)$$

where $C_{par}$ is parasitic capacitance. The cut-off frequency $f_T$ as high as 100GHz has been achieved for 0.25$\mu$m device. It is expected to be higher than 150GHz for 0.10$\mu$m device.

### 4.4 mHEMT and pHEMT Devices

Having describing the physics of AlGaAs/GaAs unstrained Structures. Let’s consider other type of MODFET namely pseudomorphic MODFET and metamorphic MODFET. In general the types of MODFET structure are shown in Fig. 4.7.

Introduction of indium in InGaAs causes lattice mismatch to the GaAs substrate since the lattice constant of InAs and GaAs are 6.07 Å and 5.64 Å respectively. However, the growth of good-quality hetero-epitaxial layer is still possible provided the epitaxial-layer thickness is under the critical thickness $t_c$

\[ t_c \approx \frac{a_e}{2\Delta} \approx \frac{a_e^2}{|a_e - a_s|} \]

where $\Delta$ is the lattice mismatch followed expression

\[ \Delta = \frac{|a_e - a_s|}{a_e} \]

$a_e$ is the lattice constant of epitaxial and $a_s$ is the lattice constant of substrate. Such technique yields a pseudomorphic InGaAs channel layer and the device is called *pseudomorphic MODFET or pHEMT*. On GaAs substrate, pHEMT can accommodate a maximum of 35% indium. On InP substrate, an unstrained conventional MODFET starts with 53% indium, and its pHEMT can contain as high as 80% indium. So MODFET performance on InP substrate is always higher since the mobility is higher. In general, pHEMT is sensitive to changes in strain during processing. Thermal strain has to be minimized to prevent relaxation of the pseudomorphic layer and introduction of dislocations that reduce the carrier mobility.
In order to get high indium content on GaAs substrate, in this scheme, a thick buffer layer of graded composition is grown on the GaAs substrate. This thick buffer layer serves to transform the lattice constant gradually from that of the GaAs substrate to whatever required for the subsequent growth of the InGaAs channel layer. In doing so, all the dislocations are contained within the buffer layer. The InGaAs channel layer is unstrained and dislocation-free. Such technique has permitted indium as high as 80%. The MODFET as the result of this process is called metamorphic MODFET or mHEMT.

Another material system for MODFET that has attracted increased interest recently is based on the AlGaN/GaN heterojunction. GaN has high energy gap (3.4eV) and is attractive for power, high temperature and high frequency applications because of a low ionization coefficient and thus high breakdown voltage. An interesting feature of the AlGaN/GaN MODFET is the additional carriers coming from the effects of spontaneous polarization and piezoelectric polarization, apart from the modulation doping, resulting in higher current capability. In some cases, the AlGaN barrier layer is undoped and excess carrier concentration relies on these polarization effects. However, AlGaN/GaN MODFET has several problems associate with it such as high dislocation densities that can have a detrimental effect on the performance of the device. The gate leakage current or the gate current collapse is another problem facing the nitride MODFET. Several device structures have been reported. The two most common structures are shown in Fig. 4.8.
2DEG is formed at the AlGaN/GaN interface. The most common buffer layer is the low-temperature-grown AlN layer and AlGaN/GaN superlattices. One of the main functions of the buffer layer is to prevent the dislocations formed at the substrate surfaces from propagating in the HFET structure. It also acts as an insulator between device and substrate. The formation of the 2DEG in the structure of Fig. 4.8 relies on the spontaneous polarization induced charge sheet. This requires that the polarity of the GaN surface should be Ga-rich. The sheet carrier densities in nominally undoped AlGaN/GaN structures can be comparable to those achievable in extrinsically doped structures, but without the degradation in mobility that can result from the presence of ionized impurities. A simple electrostatic analysis shows that the sheet carrier concentration \( n_s \) of the 2DEG at the Al\(_x\)Ga\(_{1-x}\)N/GaN heterojunction interface should be given approximately by

\[
n_s = \frac{\sigma_{\text{pol}}}{q} - \left( \frac{\varepsilon_{\text{AlGaN}}}{d_{\text{dep}}q^2} \right) (q\phi_b + E_p - \Delta E_C) + \frac{1}{2} N_d d_{\text{dep}} \tag{4.19}
\]

where \( \sigma_{\text{pol}} \) is the polarized induced charge density. The polarized induced charge density can be expressed in terms of lattice constant of GaN \( a_{\text{GaN}} \) and AlN \( a_{\text{AlN}} \), spontaneous polarization of GaN \( \mathbf{p}_{\text{GaN}}^{\text{sp},z} \) and Al\(_x\)Ga\(_{1-x}\)N \( \mathbf{p}_{\text{AlGa}_{1-x}\text{N}}^{\text{sp},z} \), and the relevant piezoelectric and electric constants for Al\(_x\)Ga\(_{1-x}\)N, \( \varepsilon_{31} \), \( \varepsilon_{33} \), \( c_{13} \) and \( c_{33} \). Thus, the polarized induced charge density is

\[
\frac{\sigma_{\text{pol}}}{q} \approx -2 \left[ q_{31} - \left( \frac{c_{13}}{c_{33}} \right) \mathbf{a}_{\text{AlN}} \right] \mathbf{a}_{\text{GaN}} - 1 \times \mathbf{p}_{\text{GaN}}^{\text{sp},z} \mathbf{p}_{\text{AlGa}_{1-x}\text{N}}^{\text{sp},z} \tag{4.20}
\]

There are two methods of fabricating AlGaN/GaN MODFET. The first method relies on depositing the ohmic contacts for the drain and the source and the Schottky contact for the gate directly on the AlGaN layer as shown in Fig.

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**Figure 4.8:** Two types of the most common AlGaN/GaN HFET structures

![Diagram of AlGaN/GaN HFET structures](image-url)
4.9(a). The second method utilizes an oxide layer, such as SiO$_2$, Al$_2$O$_3$, and silicon oxynitride, deposited underneath the gate metal, as shown in Fig. 4.9(b).

![Figure 4.9: (a) AlGaN/GaN with source, drain and gate directly deposited on surface of AlGaN (b) AlGaN/GaN with additional oxide layer](image)

The acronym MOSHFET is given to this type of HFET, which indicates a metal-oxide semiconductor MODFET. The advantage of the second method is that the gate current is reduced due to the presence of the oxide underneath the gate. An example of a top view of a GaN/AlN MODFET is shown in Fig. 4.10.

![Figure 4.10: Top view of a typical AlGaN/GaN HFET](image)

Typically the source-to-drain spacing or channel length is $L \approx 2\mu m$ and the gate length is $y \approx 5\mu m$. However, the total gate length could be as large as 50 to 200$\mu m$ and the width of the gate metal is $W_G \approx 0.2\mu m$. 

- 159 -
There are many structural variations for AlGaN/GaN HFETs. Fig. 4.11 shows three different variations. The first structure shown in Fig. 4.11 is a single heterojunction and its conduction energy band diagram. Figure 4.12 shows the double-heterojunction HFET, which is simply a single quantum well. The conduction energy band diagram shows the positive and negative charge carriers generated from the spontaneous polarization effect. A third type is shown in Fig. 4.13, which is composed of two 2DEG channels. The 2DEG is almost doubled in this structure. Additional channels can be added to further increase the 2DEG density.

**Figure 4.11:** A single heterojunction AlGaN/GaN HFET and its conduction band diagram

**Figure 4.12:** A double heterojunction AlGaN/GaN HFET and its conduction band diagram
The buffer layers in these AlGaN/GaN structures vary from structure to structure. The most common buffer layer schemes are low-temperature-grown AlN, which is a thick undoped GaN layer and Al$_x$Ga$_{1-x}$N/GaN superlattices. More complicated buffers are composed of more than one scheme, such as AlGaN/GaN superlattices sandwiched between undoped GaN layers. The superlattice-GaN layer could be repeated several times to ensure the presence of high-quality surfaces on which the device structure can be deposited.

### 4.5 Monolithic Microwave Integrated Circuit MMICs

Monolithic microwave IC MMIC technologies span a broad range of circuits range from power amplifier to mixers to transmit/receive modules. The application includes cellular phone, direct-broadcast satellite, data links, cable television CATV, radar transmission and detection, and even automobile collision avoidance system. Figure 4.14 shows a typical MMIC showing some common analog components such as metal insulator metal MIM capacitor, tuning capacitor, resistor, GaAs field effect transistor etc.

MMIC’s begins with the base metal semiconductor field effect transistor. The gate electrode is not necessary be centered-type. For power application, comb structure may be used for the gate electrode, with alternating sources and drain. The critical part here that must be designed is very short channel length knowing that the unit gain frequency is inversely proportional to the channel length. Beside this advantage, short channel length shall mean low noise figure. Consequently, current generation of MMICs has channel length of 0.1µm. Since the number of transistor count in MMICs is low. MMICs is usually fabricated with electron-beam lithography.
Many analog circuits require the use of capacitor and inductor. They are used to adjust the signal phase, to impedance match the source and load or to filter the signal. Capacitor may be formed in two ways. Interdigitated capacitor can be formed on a single layer metal but typically have capacitance of less than 1.0pF. This type of capacitor is difficult to control in terms of dimension because it is lithographically defined.

When large area or more precisely controlled capacitance is needed, an overlay capacitor can be as shown in Fig. 4.15. The common dielectric material for overlay capacitor is silicon nitride Si$_3$N$_4$, although Silicon dioxide SiO$_2$, Al$_2$O$_3$ and polyimide have been used.
There are three methods for making inductors in MMICs. Metal thickness in all three types is typically several microns thick to reduce resistivity and minimize skin loss. Straight line inductor is used for highest frequencies but typically have too low inductance in less than 1.0nH, which is suitable for most applications.

Single loop “Ω” inductors are also easy to form but limited to a few nanohenries. Spiral inductor can be made for inductance more than 50nH but requires two levels of metal with underpass. Air bridge process is often used in forming spiral inductor and typically used to minimize parasitic capacitance. The process steps are shown in Fig. 4.16. The thick polyimide is patterned on the substrate until exposed substrate. Metal deposition is made sufficiently to ensure lifting after dissolving the polyimide. Instead of using air bridge, gold air bridge can be used because of its resistivity.
Interconnect must be controlled for high frequency application. Line must be well shielded from each other to avoid cross-talk. Line loss must be minimized and finally a stable ground is needed. The microstrip waveguides method is shown in Fig. 4.17(a). It uses the back of the wafer as ground plane. Usually the wafer is thinned from 500µm to 100µm. This is done by lapping in abrasive materials such as alumina and silicon carbide. It is then polished using wet chemical. The through hole is then patterned and etched with the infrared aligner to make sure front side and backside is aligned. The deposition of gold is made with the aid of infrared red IR camera to ensure the microstrip is deposited. Coplanar waveguide is another way as shown in Fig. 4.15(b). The guide terminates the field line associated with waveguide with parallel ground. The line must wide and closed to signal line.
4.6 Optoelectronic Devices

Gallium arsenide GaAs is a direct band-gap material with energy band-gap 1.43eV ($\lambda_G = 860$nm). The radiation recombination is band to band transition. It can be used for production of light emitting diode LED and semiconductor laser.

Light emitting diode LED utilizes the principle of recombination of majority carrier in $pn$ junction to produce light, which is also termed as injection electroluminescence. Forward biasing the $pn$ junction would inject the majority carrier from each side of the $p$ and $n$ materials across the junction, whereby it will recombine with the majority carrier at the other side of the junction to produce visible light. The illustration is shown in Fig. 4.18.

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**Figure 4.17:** (a) Coplanar interconnect and (b) microstrip interconnect

**Figure 4.18:** Injection of minority carrier and subsequent radiative recombination with majority carrier in a forward bias $pn$ junction
Semiconductor laser is one of the most important light sources for optical-fiber communication. It can be used in many other applications like scientific research, communication, holography, medicine, military, optical video recording, optical reading, high speed laser printing etc. In order to produce laser, the semiconductor should be the direct semiconductor and the doping concentration of the junction should be higher than the effective density of state of the said semiconductor material. In another word, the material should be a degenerate semiconductor.

Figure 4.19 shows three laser structures. The first structure is a basic $pn$ junction laser called a homojunction laser shown in Fig. 4.19(a) because it has the same semiconductor material such GaAs. A pair of parallel plane or facets are cleaved or polished perpendicular to the (110) axis. Under appropriate biasing condition, laser light will be emitted from these planes (only the front emission is shown). The two remain sides of the diode are roughened to eliminate lasing in the direction other than the main ones. This structure is called *Fabry-Perot cavity* with typical length cavity $L$ of about $300\mu$m. This type of cavity is extensively used in modern semiconductor laser.

Figure 4.19(b) shows the double heterojunction structure laser, which has a thin layer of semiconductor such as GaAs sandwiched between layers of a different semiconductor such as $Al_{x}Ga_{1-x}As$. The homojunction and double heterojunction lasers are broad-area laser because the entire area along the junction plane can emit radiation. Figure 4.19(c) shows the double-heterojunction laser with strip geometry. The strip width $S$ is typically $5-30\mu$m. The advantages of the strip geometry are reduced operating current, elimination of multiple-emission area along the junction, and improved reliability that is result of removing most of the junction perimeter.
Figure 4.19: Semiconductor laser structure in Fabry-Perot cavity configuration (a) Homojunction laser, (b) double-heterojunction laser DH, and (c) stripe-geometry double-heterojunction laser

The structure of quantum-well QW laser shown in Fig. 4.20 is similar to the double-heterojunction DH laser except the thickness of the active layer in a QW laser is very small typically about 10-20nm sandwiched between two large band-gap AlGaAs. It can emit laser with 900nm wavelength. The length $L_y$ is comparable to de Broglie wavelength and the carriers are confined in a finite potential well in y-direction. The energies of electron and hole are separated into confinement components in the y-direction and two unconfined in the x- and z-directions. According Schrödinger's wave equation with the boundary conditions applied to the quantum well, the energy confinement component is defined as
Alternative Device Structures

\[ E(n,k_x,k_z) = E_n + \frac{\hbar^2}{2m^*_n}(k_x^2 + k_z^2) \]  

(4.21)

where \( E_n \) is the \( n \)th eigenvalue of the confined particle, \( m^*_n \) is the effective mass, and \( k_x \) and \( k_z \) are the wave number in the x and z-directions respectively. Figure 5.13(a) shows the energy level of quantum well. The value of \( E_n \) are shown as \( E_1, E_2, E_3 \) for electrons, \( E_{hh1}, E_{hh2}, E_{hh3} \) for heavy hole, and \( E_{lh1}, E_{lh2} \) for light holes. The usual parabolic forms for the conduction and valence band density of states have been replaced by a ‘staircase’ representation of discrete levels as shown in Fig. 4.20. Each level corresponds to a constant density of states per unit area given by equation (4.22).

\[ \frac{dN}{dE} = \frac{m^*}{\pi \hbar^2} \]  

(4.22)

Figure 4.20: The quantum-well laser

Since the density of state is staircase form and constant rather than continuous type for the case of conventional type of 3-dimensional semiconductor. This group of electron of nearly same energy can combine with a group of hole of near same energy. For an example, the level \( E_1 \) in conduction band combines with the level \( E_{hh1} \) in the valence band. This makes QW laser much better performance like reduction in threshold current, high output power, and high speed as compared with conventional DH laser. QW laser makes from GaAs/AlGaAs material has threshold current density as low as 65A/cm² and
sub-milliampere threshold current. The laser operates at emission wavelength around 0.9µm.

For long wavelength operation, GaInAs/GaInAsP multiple-quantum-well MQW laser with wavelength 1.3µm and 1.5µm regions have been developed. Figure 4.21(a) shows a schematic diagram of separate-confinement-heterostructure SCH MQW laser where four QWs of GaInAs with GaInAsP barrier layers are sandwiched between the InP cladding layers to form a waveguide with step index change. These alloy compositions are chosen so that they are lattice matched with the InP substrate. The active region is composed of four 8nm thick, undoped GaInAs QWs with $E_G = 0.75$eV separated by 30nm thick undoped GaInAsP layers with $E_G = 0.95$eV. Figure 4.21(b) shows the corresponding energy band diagram of the active region. The $n$- and $p$-cladding InP layers are doped with sulfur ($10^{18}$ cm$^{-3}$) and zinc ($10^{17}$ cm$^{-3}$) respectively.

A graded-index SCH (GRIN-SCH) shown in Fig. 4.21(c), in which a GRIN of waveguide is accomplished by several small stepwise increases of band-gap energies of multiple cladding layers. The CRIN-SCH structure confines both the carriers and the optical field more effectively than the SCH structure and consequently leads to an even lower-threshold current density. With MQW structure, a variety of advanced lasers and photonic integrated circuits becomes possible for future system applications.

![Diagram of MQW laser structure](image)
4.7 Heterojunction Bipolar Junction Transistor

The $\alpha$ and $\beta$ of a homojunction bipolar junction transistor is equal to $\alpha = B\gamma_e = B\frac{I_{En}}{I_{En} + I_{Ep}}$ and $\beta = \frac{B\gamma_e}{1 - B\gamma_e}$, where $B$ is the base transport factor, $I_{En}$ is the majority emitter current, $I_{Ep}$ is the minority emitter current, and $\gamma_e$ is the emitter efficiency. Thus, traditional design of homojunction bipolar transistor has to reduce the concentration of base and increase the doping concentration of emitter in order to achieve high emitter efficiency. However, increase concentration of emitter means reducing speed due to larger capacitance and reducing doping concentration of the base means increase the transist time.

A transistor made with heterojunction material, its emitter efficiency can be increased without strict requirement on the doping concentration. As shown in Fig. 4.22, the built-in potential $qV_{\text{bin}}$ for electron and hole $qV_{\text{bip}}$ are the same for homojunction bipolar junction transistor, whilst $qV_{\text{bin}}$ is lower than $qV_{\text{bip}}$ for an $npn$ heterojunction bipolar junction transistor that uses a wide band-gap emitter such as $\text{Al}_x\text{Ga}_{1-x}\text{As}$ and narrow energy band-gap base such $\text{GaAs}$. Since the carrier injection varies exponentially with built-in potential, even a small difference in these two built-in potentials can make a very large difference in the transport of electron and hole across the emitter junction. Knowing that the minority carrier for homojunction $n$-type emitter is $p_\text{eo} = n_i^2/N_{De}$. For a heterojunction $n$-type emitter, the minority carrier $p_\text{eo}$ depending on an additional exponential term, which is

$$p_\text{eo} = \frac{n_i^2}{N_{De}} \exp\left(-\frac{\Delta E_G}{kT}\right)$$

(4.23)
where \( \Delta E_G = E_{Ge} - E_{Gb} \).

The additional term \( \Delta E_G \) in equation (4.23), which is the difference between wide band-gap emitter and narrow band-gap base, allows choosing lightly doped emitter for reducing junction capacitance and heavily doped base to reduce base resistance freely without affecting the emitter efficiency.

For a small \( \Delta E_G \) of 0.4eV like the case of \( \text{Al}_{0.3}\text{Ga}_{0.7}\text{As} \) and \( \text{GaAs} \) emitter-base junction, the value of minority hole in emitter \( p_{eo} \) is at least \( 1 \times 10^{11} \) time smaller than the \( p_{eo} \) of homojunction BJT. This implies that the emitter efficiency is essentially unity, so do \( \alpha \) and \( \beta \) values would be improved.

Thus, using this approach it does not scarify operation speed of the device. A basic heterojunction bipolar junction transistor utilizing \( n-\text{Al}_x\text{Ga}_{1-x}\text{As}/P^+\text{-GaAs}/n^+\text{-Al}_x\text{Ga}_{1-x}\text{As} \) is shown in Fig. 4.23.
The minority carrier concentration in the emitter and base of an \textit{npn} HBT are given by equation (4.24) and (4.25).

\begin{equation}
 p_{eo} = \frac{n_{ie}^2}{N_{De}} = \frac{N_{Ge} N_{Ve}}{N_{De}} \exp \left( \frac{-E_{Ge}}{kT} \right) \tag{4.24}
\end{equation}

\begin{equation}
 n_{bo} = \frac{n_{ib}^2}{N_{Ab}} = \frac{N_{Ch} N_{Vb}}{N_{Ab}} \exp \left( \frac{-E_{Gb}}{kT} \right) \tag{4.25}
\end{equation}

The current gain is $\beta \approx \frac{n_{bo} D_{b} L_{e}}{p_{eo} D_{e} W_{bn}} \approx \frac{n_{bo}}{p_{eo}}$ for the homojunction transistor. The current gain $\beta$ for heterojunction transistor shall be

\begin{equation}
 \beta = \frac{N_{Ch} N_{Vb}}{N_{Ab}} \frac{N_{De}}{N_{Ge} N_{Ve}} \exp \left( \frac{E_{Ge} - E_{Gb}}{kT} \right) \approx \frac{N_{De}}{N_{Ab}} \exp \left( \frac{\Delta E_{G}}{kT} \right) \tag{4.26}
\end{equation}

where $\Delta E_{G} = E_{Ge} - E_{Gb}$.

InP/InGaAs heterostructure has very low surface recombination and higher electron mobility in InGaAs than GaAs. Thus, InP-based HBT has high cut-off frequency and as high as 254GHz has been obtained. The InP collector region has higher drift velocity than GaAs collector at high electric field and it has high breakdown voltage than gallium arsenide GaAs.

The structure of an \textit{npn} Si/SiGe/Si HBT is shown in Fig. 4.24. Si/SiGe/Si has a higher current gain $\beta$ as compared to homojunction Si transistor. Comparing with InP-based HBTs, it has lower cut-off frequency due to lower mobility.

![Figure 4.24: A Si/SiGe/Si heterojunction transistor](image-url)
Exercises

4.1. Name two advantages of GaAs technologies over CMOS technologies.

4.2. A GaAs MESFET with gold Schottky barrier of barrier height 0.8V has $n$-channel doing concentration $2.0 \times 10^{17} \text{ cm}^{-3}$ and channel thickness 0.25μm. Calculate the threshold voltage for this MESFET.

4.3. A GaAs MESFET has channel mobility $\mu_n = 6,000 \text{ cm}^2/\text{V-s}$, Schottky barrier height $\phi_b = 0.8V$, channel depth $h = 0.25 \mu\text{m}$, channel doping concentration $N_D = 8.0 \times 10^{16} \text{ cm}^{-3}$, channel length $L = 2.5 \mu\text{m}$ and gate width $W = 30 \mu\text{m}$. Calculate the saturation current and transconductance when gate voltage of 0.0V and - 0.5V applied to it.

4.4. Consider an $n$-channel GaAs MESFET that has ideal saturation current $4.03 \text{mA}$ at $V_{DSSAT} = 3.0V$, channel length $2.0 \mu\text{m}$, and doping concentration $5.0 \times 10^{16} \text{ cm}^{-3}$. What is the channel resistance of the device for $V_{DS}$ change from 3.1V to 3.2V?

4.5. The energy band diagram of $n^+\text{-Al}_{0.3}\text{Ga}_{0.7}\text{As}/n\text{-GaAs}$ heterojunction is shown in the figure. Calculate the delta energy band-gap and electron affinity of Al$_{0.3}$Ga$_{0.7}$As.

4.6. Describe the requirements needed to design semiconductor laser in terms of type and semiconductor and doping concentration.
Bibliography