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Chapter 1

Introduction to Microelectronic Fabrication

1.0 Introduction

Jack Kilby was the first person to develop miniaturized transistor circuit in 1958. It was then followed by Robert Noyce and Gordon Moore, who built first planar miniaturized transistor in 1960. Thereafter, with the aid of computer and advancement in lithography, integrated circuit IC was fast developed into ultra large scale integration ULSI where billions of transistors can be built in a silicon chip of 3.0cm x 3.0cm area.

Integrated circuit is built mainly on silicon due to cheap, developed processes, and abandon on the earth crust. Beside these reasons, the byproduct produced by the process is not toxic and can be disposed easily. There are many other available materials that can be used to build integrated circuit. They are gallium arsenide GaAs, silicon carbide SiC, gallium nitride GaN, silicon germanium SiGe and etc. Unless, it is mentioned, this lecture shall be presented using silicon as the building element for the integrated circuit.

An integrated circuit IC consists of a single crystalline chip or it may be called monolithic, typically 300µm to 600µm thick and covering a surface area of 3.0cm x 3.0cm containing both active and passive elements.

The fabrication of integrated circuit IC both MOS, bipolar devices, and other devices involves a numbers of repeated major process steps. The processes can be broadly classified into wafer cleaning process, photolithography (imaging, resist-bleaching and resist development), oxidation process, etching, diffusion/ion implantation, chemical vapor deposition CVD for thin film deposition, epitaxial silicon and polycrystalline process, physical vapor deposition/metal deposition or evaporation/sputtering, thin film such as silicon nitride Si₃N₄, titanium nitride TiN, titanium tungsten Ti-W alloy, titanium silicide TiSi₂, tungsten silicide WSi₂ processes, and sintering/rapid thermal annealing RTA.

Semiconductor such germanium, silicon, and gallium arsenide have a lattice structure consisting of two interlocking face-centered cubic lattices, and have total of eight atoms per unit cell. This structure can be broken down into
primitive cell of tetrahedral shape shown in Fig. 1.1 and diamond structure shown in Fig. 1.2. Diamond structure has different atom type such as gallium arsenide is called zinc blende.

The most common two types of silicon crystal orientations used to fabricate the integrated circuit are (111) and (100) types. The selection of the type depends on the type circuit to be built. (111) orientation is widely used for fabricating bipolar device, whilst (100) type is mainly used to fabricate MOSFET. (100)-type has the surface state charge 30-40% less than (111) type. Thus, it is ideal to use for MOSFET fabrication in which the device is sensitive to surface trapping and thereby affecting the mobility of the device. Bipolar device is a current...
driven device. Thus, surface state charge would not have significant impact on the speed of the device. Moreover, choosing the right orientation would assist scribing in dicing of the silicon wafer. Figure 1.3 shows one of the common ways to identify the orientation and dopant type. Other way to identify the orientation and dopant type is by mean of notch.

![Diagram showing wafer flats for identifying orientation and dopant type](image)

**Figure 1.3**: Wafer flat for identifying the orientation and dopant type

In this chapter, we discuss the semiconductor materials, semiconductor devices, the processes of fabrication of integrated circuits including the process of silicon crystal growth, clean room requirements, and gettering process of eliminating contaminants.

### 1.1 Semiconductor Materials

Semiconductor materials can be classified into many types. They are elemental semiconductor, compound semiconductor, narrow band-gap semiconductor, wide band-gap semiconductor, oxide semiconductor, magnetic semiconductor, polysilicon semiconductor, amorphous semiconductor, organic semiconductor, low dimension semiconductor, and etc. We shall discuss the important type and a few other types.
1.1.1 Elemental Semiconductor

Silicon Si, germanium Ge, and diamond C are important group IV elemental semiconductors. These group IV elemental materials have diamond crystal structure. Another group IV elemental semiconductor having such a structure is alpha tin $\alpha$-Sn, which is also referred as gray Sn. Other elemental structures differing from diamond structure include group III element boron (Rhombohedral), group V material phosphorus, and group VI materials such as sulphur S, selenium Se, and tellurium Te.

Currently silicon Si is the most important semiconductor material used in electronic devices. Some of the important advantages of silicon Si over other semiconductors are:

- A relative ease of passivating the surface by oxidizing in a controlled manner forming a layer of stable native oxide that substantially reduces the surface recombination velocity.
- It has hardness for making large wafers that can be handled safely without damaging it.
- It is thermally stable up to $1,100^\circ$C that allows high-temperature processes like diffusion, oxidation, and annealing.
- It is relatively low cost due to established processes.

The basic limitations of silicon Si are the magnitude and type of its energy band-gap. Its energy band-gap is $1.12\text{eV}$. It is an indirect semiconductor that limits the application in optoelectronics and it has relatively low carrier mobility as compared to other semiconductor such as gallium arsenide GaAs.

Emerging materials based on Si nanostructures e.g., Si nanocrystals, quantum wires and dots, and porous Si, and $\text{Si}_x\text{Ge}_{1-x}$ layers grown on Si substrate, appear to be promising materials in various applications. In nanostructures because of quantum confinement of carriers, it leads to increase of electron hole wave function overlap and hence, it increases photon emission efficiency. There is a high-energy shift toward the emission blue peak.

Porous Si can be obtained from the anodic etching of crystalline Si in aqueous hydrofluoric acid HF. It contains a network of pores and crystallites (microscopic crystal) with sizes in the order of several nanometers. This material exhibits relatively efficient luminescence, which is several orders of magnitude higher than that in crystalline Si, and it is believed to be related to the quantum confinement effects in nanocrystalline Si.
1.1.2 Compound Semiconductor

There are many compound semiconductor materials. They are usually formed from III-V group, II-VI, IV-VI, I-III-VI₂ elements. III-V group semiconductors are GaAs, GaP, GaN, AlAs, InSb, InAs, InP and etc. In general, these crystallized materials have relatively high degree of stoichiometry (chemistry deal with the relative quantities of reactants and products in chemical reactions). Many of these compounds such as GaAs, InAs, InP, and indium antimonide InSb have direct energy band-gaps and high carrier mobilities. Thus, the common applications of these semiconductors are used to design a variety of optoelectronic devices for both the detection and generation of electromagnetic radiation, and also in high-speed electronic devices. The energy band-gaps of these compounds are useful for optoelectronic applications. The energy band-gap ranges from 0.17eV for InSb to 3.44eV for GaN covering the wavelength range from about 7.29 to 0.36μm, which is from infrared through visible and to ultraviolet spectral ranges. Materials such as GaAs and InP are also extensively used as substrates for a wide variety of electronic and optoelectronic devices such as light-emitting devices.

II-VI compound semiconductor such as Zn and Cd-chalcogenides such as compounds with oxygen O, S, Se, and tellurium Te cover a wide range of electronic and optical properties due to the wide variations in their energy band-gap. These compounds are also relatively easily miscible (can be mixed well in any proportion), which allows a continuous “engineering” of various properties. However, the preparation of high-quality materials and the processing technologies are not sufficiently developed in comparison with those related to silicon Si and some III-V compounds. The II-VI compounds are typically n-type as grown, except ZnTe, which is p-type. Among these compounds, the conductivity type of CdTe can be changed by doping, and thus n- and p-type materials can be obtained. Others II-VI compound such as ZnSe, ZnS and CdS can be doped to produce a small majority of holes. For device applications, it is possible to form heterojunctions in which the n- and p-sides of the junction are of different II-VI compound semiconductors, and to use metal-semiconductor and metal-insulator-semiconductor structures for carrier-injection device applications. All the II-VI compound semiconductors have direct energy band-gaps, thus, high efficient emission or absorption of electromagnetic radiation can be expected from these materials. Therefore, these semiconductors are important mainly for their optical properties. In addition to the binary II-VI compounds, materials such as ternary compound like Zn₁₋ₓCdₓS and ZnSₓSe₁₋ₓ, and quaternary compound such as Zn₁₋ₓCdₓSₓSe₁₋ₓ alloys with “engineered” properties are also of interest.
IV-VI compound semiconductor like lead chalcogenides such as PbS, PbSe, and PbTe are characterized by narrow energy gaps, high carrier mobilities, and high dielectric constants. The unique feature of the direct energy gap in these compounds is that its energy band-gap increases with increasing temperature, which means the energy gap has a positive temperature coefficient, PTC. In contrast to the temperature behavior of the energy band-gap in other elemental and compound semiconductors, they have a negative temperature coefficient. Main applications of these compounds are in light-emitting devices and detectors in the infrared spectral region.

I-III-VI₂ chalcopyrite compound semiconductor such as CuAlS₂, CuGaS₂, and CuInSe₂ are direct semiconductors that have energy band-gaps between 1.0eV to 3.5eV. In addition, CuAlS₂, CuGaS₂ can be made into p-type which is suitable for making heterojunction with wide energy band-gap n-type II-VI compound semiconductor. Some possible applications of this compound semiconductor are light emitting device and photovoltaic solar cells.

1.1.3 Narrow Band-gap Semiconductor

Narrow band-gap semiconductors such as InSb, InAs, PbSe have the energy band-gap below about 0.5eV. Such semiconductors are extensively employed in such infrared optoelectronic device applications as detectors and diode lasers.

Photoconductive lead sulphide PbS and lead selenide PbSe detectors can be employed in the spectral range between about 1.0 and 6.0µm. Another important material used as a detector in the infrared range is Hg₁₋ₓCdₓTe.

1.1.4 Wide Band-gap Semiconductor

Wide band-gap semiconductor is also referred as refractory semiconductors since they are employed in high temperature application. The typical types of this semiconductor are SiC and II-V nitrides that have high thermal conductivity, high saturation electron drift velocity, high breakdown electric field, and superior chemical and physical stability. The semiconductor has high thermal conductivity indicates it can be used in high temperature at high power level operation. It has wide band-gap that enables detection and emission of light in short-wavelength region likes blue and ultraviolet. It has high saturation electron drift velocity that can be used in radio frequency RF and microwave operations. High breakdown electric field enables the realization of high power electronic devices and also allows high device packing density for integrated circuit.
1.1.5 Oxide Semiconductor

Oxide semiconductors are also referred as semiconductor ceramics. These materials are polycrystalline and polyphase materials with grain sizes in the range between 1.0 to 10.0μm. The properties of grains and grain boundaries play a crucial role in both the understanding and application of the materials. Some examples of oxide semiconductors are Cu$_2$O (2.1eV), Bi$_2$O (2.8eV), ZnO (3.4eV) etc. They are used in electronic devices and sensors such as positive temperature coefficient PTC thermistor, varistor - resistor with non-linear but symmetric current-voltage characteristics, capacitor of high dielectric constant, gas sensor, and electro-optic modulators.

1.1.6 Magnetic Semiconductor

Semiconductor compound contains magnetic ions such as Cr, Mn, iron Fe, Co, nickel Ni, and europium Eu may exhibit magnetic properties. Some oxides such as FeO and NiO exhibit anti-ferromagnetic properties and oxide such as europium oxide EuO and EuS are ferromagnetic properties. The semiconductor exhibits large magneto-optical effect that can be used to design optical modulators.

There are many other semiconductor types such as amorphous semiconductor and organic semiconductor that are not discussed. Student may take your own initiative to study on your own.

1.2 Semiconductor Devices

Semiconductor devices are electronic components that exploit the electronic properties of semiconductor materials, principally silicon, germanium, and gallium arsenide, organic semiconductors, and other semiconductors. Semiconductor devices have replaced thermionic devices (vacuum tubes) in most applications. They use electronic conduction in the solid state as opposed to the gaseous state or thermionic emission in a high vacuum.

Semiconductor devices are manufactured both as single discrete device and as integrated circuits ICs, which consist of a number from a few devices to billions of devices manufactured and interconnected on a single semiconductor substrate.

Semiconductor materials are so useful because their behavior can be easily manipulated by the addition of impurities. Semiconductor conductivity can be
controlled by introducing electric or magnetic field, by exposure to light or heat, or by mechanical deformation of a doped monocrystalline grid. Current conduction in a semiconductor occurs via mobile or free electrons and holes, collectively known as charge carriers. Doping a semiconductor with a small amount of impurity atoms, such as phosphorus or boron, greatly increases the number of free electrons or holes within the semiconductor. When a doped semiconductor contains excess holes it is called *p*-type, and when it contains excess free electrons it is known as *n*-type. The semiconductor material used in devices is doped under highly controlled conditions in a fabrication facility to precisely control the location and concentration of *p*-type and *n*-type dopants.

Many semiconductor devices had been invented in last 60-70 years since the day first transistor was built in Bell laboratory in 1947. We shall spend sometimes in this section briefly describe some common semiconductor devices used today. They are *pn* junction or diode, bipolar junction transistor, MOSFET, MESFET transistor, and MODFET transistor.

### 1.2.1 PN Junction

PN junction is of great importance both in modern electronic application and in the understanding of other semiconductor device. It is the simplest form of homojunction formed by doping *p*-type impurity and *n*-type impurity into a single crystal intrinsic semiconductor. It shows a very interesting behavior of electrons and holes in the junction. William Shockley was the first person established the basic theory of current voltage characteristics of *pn* junction and this had served as the foundation for establishing other semiconductor theories. *pn* junction conducts high current in one direction and conduct very small amount of current in the reversed direction. Thus, *pn* junction has the property of rectification.

The total charge of a *pn* junction is given by equation (1.1).

\[
Q = A \left[ 2q \varepsilon_s (V_{th} + V_R) \frac{N_D N_A}{(N_A + N_D)} \right]^{1/2}
\]

(1.1)

If abrupt junction is assumed at the *n*-type region and \(N_D \gg N_A\) then \((N_A + N_D)\) is \(\approx N_D\). The capacitance of the *pn* junction is given by equation (1.2).

\[
C_j = \left[ \frac{q \varepsilon_s N_A}{2(V_{th} + V_R)} \right]^{1/2}
\]

(1.2)
where $V_{bi}$ is the built-in potential and is equal to $V_{bi} = \frac{kT}{q} \ln \left( \frac{N_A N_D}{n_i^2} \right)$.

If equation (1.2) is rearranged, it becomes

$$\left( \frac{1}{C_j} \right)^2 = \frac{2(V_{bi} + V_R)}{q\varepsilon_s N_A}$$

(1.3)

From the graph of $1/C_j^2$ versus applied voltage $V_R$, the concentration of impurity $N_D$ and $N_A$ can be obtained from the gradient of the plot and from the intersection at applied voltage axis by the gradient, the built-in potential $V_{bi}$ can be obtained. The capacitance of the junction can be measured by applying a few milli-volt of ac signal with in frequency in 100kHz range, riding on a sweeping dc voltage to one end of the junction. The output at the other junction is dc filtered and fed into the lock-in amplifier to measure the capacitive component and conductive component.

The ideal current-voltage current density of a $pn$ junction is governed by equation (1.4).

$$J = \left[ \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{po}}{L_n} \right] \exp \left( \frac{qV_R}{kT} \right) - 1$$

(1.4)

where the reverse saturation current density is $J_S = \left[ \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{po}}{L_n} \right]$, where $D_p$, $D_n$, $p_{no}$, and $n_{po}$ are the diffusion coefficient of minority hole, diffusion coefficient of minority electron, minority hole in $n$-region, and minority electron in $p$-region at equilibrium.

Equation (1.4) becomes equation (1.5) after replacing $\left[ \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{po}}{L_n} \right]$ with $J_S$.

$$J = J_S \left[ \exp \left( \frac{qV_R}{kT} \right) - 1 \right]$$

(1.5)
When the \( pn \) junction is under reversed bias, the applied voltage becomes \( -V_R \). Expression \( \exp\left(\frac{qV_R}{kT}\right) \) in equation (1.5) shall be approaching zero for \( |V_R| \gg \frac{kT}{q} \). Thus \( J = -J_S \) when the \( pn \) junction is under reverse bias and current density is independent of the biased voltage to a certain extend. Figure 1.4 shows the current density \( J \) versus applied voltage \( V_R \) of \( pn \) junction.

![Figure 1.4: Current-voltage characteristic of a \( pn \) junction](image)

**1.2.2 Bipolar Junction Transistor**

Bipolar junction transistor BJT was invented in 1948 by John Bardeen and Walter Brittain. The principle of operation was explained by W. Shockley a year later. Bipolar junction transistor is a three terminal semiconductor device used primarily for signal amplification and as switching device. It is also formed the fundamental element for integrated circuit design such as the VLSI microprocessor.

Bipolar junction transistor can be viewed as two \( pn \) junctions connected back to back to form \( np-pn \) or \( pn-np \) structures name as \( nnp \) or \( pnp \) transistor. Figure 1.5 shows a structure of a bipolar junction transistor showing presence of two \( pn \) junctions.
Figure 1.5: The structure of a bipolar junction transistor showing two \( pn \) junctions

Like \( pn \) junction the current components of bipolar junction transistor come from two carrier types, which are the hole and electron current. This is also the reason why it is called \textit{bipolar} device.

The current components shown in Fig. 1.6 are diffusion hole, diffusion electron, drift hole, and drift electron, which already reviewed in theory of \( pn \) junction.

Figure 1.6: Illustration of the current components of a \( p^+np \) transistor

Bipolar junction transistor has three terminals. One terminal is used to inject carrier name as emitter E, one is used to control the passage of the carrier named as base B, and one is used to collect the carrier named as collector C.

Bipolar junction transistor is designed in such that the doping concentration of its emitter is higher than the doping concentration of the base and collector. The order of doping concentration is highest for emitter \( \sim 10^{18} \text{cm}^{-3} \), followed by collector \( \sim 10^{17} \text{cm}^{-3} \) and than base \( \sim 10^{16} \text{cm}^{-3} \). This is to ensure closed to 100%
of the injected carrier are collected by collector. The diffusion carriers of emitter have to outnumber the recombination of carrier in the base.

The base is also designed to be much shorter than the diffusion length $L_p$, or $L_n$ of the minority hole or electron carriers.

In normal operation of bipolar junction transistor, the emitter-to-base junction of the bipolar junction transistor is always forward biased. The collector-to-base is always reverse-biased which is shown in Fig. 1.7 for $n^+pn$ bipolar junction transistor.

Biasing emitter-to-base of bipolar junction transistor will inject majority electron carrier into the $p$-base. Some of the electrons will recombine with the majority hole carriers in the base to form part of the base current $I_B$. Most of the minority electron carrier will reach the depletion edge in the collector and being swept to form collector current $I_C$. Since the injected minority electron carriers are due to emitter current, therefore the collector current $I_C$ is $BI_{En} + I_{Gen} + I_{Cn} + I_{Cp}$, which is approximately equal to equation (1.6) since generation current $I_{Gen}$ and drift hole current $I_{Cp}$ and drift electron current $I_{Cn}$ at collector are very small.

$$I_C = BI_{En}$$

where $I_{En}$ is the electron current of the emitter. The factor $B$ is called the base transport factor and its value is less than one. The emitter current $I_E$ is made up of two components, which are injected electron $I_{En}$ from $n^+$ to $p$-region and hole injected current $I_{Ep}$ from $p$ to $n^+$ region.

Thus, we can define the efficiency $\gamma_e$ of the emitter as
For efficient bipolar junction transistor both $B$ and $\gamma_e$, values must be close to unity. The ratio of collector current $I_C$ and emitter current $I_E$ shall be

$$\frac{I_C}{I_E} = \frac{BI_{En}}{I_{En} + I_{Ep}} = \frac{BI_{En}}{I_{En} + I_{Ep} - BI_{En}} = \frac{BI_{En}}{I_{En} - BI_{En}}$$

$$= \frac{B(I_{En} / I_{E})}{1 - B(I_{En} / I_{E})} = \frac{B\gamma_e}{1 - B\gamma_e} = \frac{\alpha}{1 - \alpha} = \beta \tag{1.9}$$

where $\beta$ is called the base to collector current amplification factor. The factor $\beta$ can be quite large for BJT.

The collector current $I_C$ is approximated from equation (1.10).

$$I_C \approx An_p q v_n \approx An_p \frac{q W_b}{\tau_t} \tag{1.10}$$

where $A$ is the cross sectional area of the device, $n_p$ is the minority concentration in $p$-base, which is the injected electron concentration from emitter into base. $\tau_t$ is the transit time of electron to pass through the base region of thickness $W_b$. $v_n$ is the electron velocity through the base, which is also equal to $W_b / \tau_t$.

The base current $I_B$ is primarily due to recombination of injected electron with majority carrier of the base. Thus,

$$I_B = \frac{A q W_b n_p}{\tau_B} \tag{1.11}$$

where $\tau_B$ is the diffusion time of the injected electron with the hole in the base. Combining equation (1.10) and (1.11) will yield
Thus, a high current gain entails a low recombination rate, which means a long diffusion time $\tau_B$. For indirect semiconductor material like silicon and germanium, their recombination time is in microsecond. For direct semiconductor such as GaAs and InGaAs, its recombination time is in the range of nanosecond. For high current gain, the material needs a very short transit time $\tau_t$. Of course, this is would benefit the speed of the device.

1.2.3 Metal Oxide Semiconductor Field Effect Transistor

The tremendous advancement of silicon technology developed in last fifty years has given advantage edge to fabricate the electronic devices. This is also due to the presence of a high quality silicon dioxide, which can be formed on silicon. It has high degree of perfection that silicon has overtaken germanium, which was the initial choice for transistors. Also due to perfection of Si-SiO$_2$ interface system that gives the reason the potential effect transistor PET like bipolar junction transistor has been replaced by field effect transistor FET in many applications in last four decades.

The MOSFET is the main member of the family of field-effect transistors. A transistor in general is a three-terminal device where the channel resistance between two of the contacts is controlled by the third terminal, which is the gate. MOSFET also has fourth terminal as contact to the substrate. The substrate is usually biased with either $V_{DD}$ voltage or $V_{SS}$ voltage depending on the type of substrate.

A family tree of field-effect transistors is shown in Fig. 1.8. The three first-level main members are insulated-gate field effect transistor IGFET, junction field effect transistor JFET and metal-semiconductor field effect transistor MESFET. They are distinguished by the way the gate capacitor is formed. In an IGFET, the gate capacitor is an insulator. In a JFET or a MESFET, the capacitor is formed by the depletion layer of a $pn$ junction or a schottky barrier respectively. In the branch of IGFET, it can be further divided into MOSFET/MISFET and heterojunction field effect transistor HFET. In the HFET branch, the gate material is a high band-gap semiconductor layer grown as a heterojunction, which acts as an insulator. Although MOSFETs have been made with various semiconductors such as Ge, Si, and GaAs, and use various oxides and insulators such as SiO$_2$, silicon nitride Si$_3$N$_4$, and Al$_2$O$_3$, the most-important system is still the SO$_2$-Si interface system.
A MOSFET essentially consists of a MOS capacitor and two diffused or implanted regions that serve as ohmic contacts to an inversion layer of free charge carriers with the semiconductor-silicon dioxide interface. Figure 1.9 illustrates the 2-D structure of an \( n \)-channel MOSFET.

The linear current of the MOSFET is governed by equation (1.13).

\[
I_{DS} = \frac{W \mu_C C_{ox}}{L} \left( V_{GS} - V_t \right) V_{DS} - \frac{V_{DS}^2}{2} \quad (1.13)
\]

One can see that the linear current is dependent on the aspect ratio of the device, which is dimensional dependence.
After pinch-off, $I_{DS}$ is assumed to be constant. The $V_{DSSAT}$ is equal to $(V_{GS} - V_t)$. Thus, the current is governed by equation (1.14).

$$I_{DSSAT} = \frac{W\mu C_{ox}}{L} \left( (V_{GS} - V_t)^2 - \frac{(V_{GS} - V_t)^2}{2} \right)$$

This is the equation for the saturation region of the MOSFET characteristics.

A typical ideal characteristic curve of an $n$-channel MOSFET is shown in Fig. 1.10. The curve shows three regions of the characteristic, which are the linear, saturation, and cutoff regions.

**Figure 1.10:** Characteristic curve of MOSFET

1.2.4 Metal Semiconductor Field Effect Transistor

The 3-D structure of a typical mesa isolated gallium arsenide GaAs metal semiconductor field effect transistor MESFET is shown in Fig. 1.11. The
internal pinch off voltage $V_p$ is equal to $(V_{bi} - V_G)$, which is also called *intrinsic pinch off voltage*. It is defined as

$$V_p = \frac{qN_D h^2}{2\varepsilon_s} \quad (1.15)$$

where $h$ is the thickness of the channel. The gate voltage $V_G$ required to cause pinch off is denoted by threshold voltage $V_t$, which is when gate voltage $V_G$ is equal to $V_t$, i.e. $V_t = (V_{bi} - V_p)$. If $V_{bi} > V_p$, then the $n$-channel is already depleted. It requires a positive gate voltage to enhance the channel. If $V_{bi} < V_p$, then the $n$-channel requires a negative gate voltage to deplete.

The gate voltage $V_G$ needed for pinch off for the $n$-channel MESFET device is

$$V_t = V_{bi} - V_p = \phi_b - \frac{kT}{q} \ln \left( \frac{N_C}{N_D} \right) - \frac{qN_D h^2}{2\varepsilon_s} \quad (1.16)$$

where $\phi_b$ is schottky barrier potential, which is defined as $\phi_b = \phi_m - \chi_s$. $\phi_m$ and $\chi_s$ are metal work function and electron affinity of semiconductor. $N_C$ is the effective density of state in conductor band of the semiconductor respectively. For GaAs semiconductor, the value of $N_C$ is $4.7 \times 10^{17} \text{cm}^{-3}$.

Like the MOSFET device, the current characteristics of the MESFET have the linear and saturation values, which are governed by the equation (1.17) and (1.18) respectively.
01 Introduction to Microelectronic Fabrication Preparation

\[
I_D = \frac{q \mu_n N_D Wh}{L} \left\{ V_D - \frac{2 [(V_D + V_{bi} - V_G)^{3/2} - (V_{bi} - V_G)^{3/2}]}{3(qN_D h^2 / 2 \varepsilon_n)^{3/2}} \right\}
\]  

(1.17)

for \(0 \leq V_D \leq V_{Dsat}\) and \(V_P \leq V_G \leq 0\).

\[
I_{Dsat} = g_o \left\{ \frac{V_p}{3} - V_{bi} + V_G + \frac{2(V_{bi} - V_G)^{3/2}}{3V_p^{3/2}} \right\}
\]  

(1.18)

for \(V_D \geq V_{Dsat}\) and \(V_G \leq V_P\). \(g_o\) is the channel conductance, which is defined as \(g_o = \frac{q \mu_n N_D Wh}{L}\).

1.2.5 Modulation Doping Field Effect Transistor

In order to maintain high transconductance for MESFET devices, the channel conductance must be as high as possible, which can be seen from equation (1.17) and (1.18) for MESFET device. The channel conductance is dependent on the mobility and doping concentration. But increasing doping concentration would lead to degradation of mobility due to scattering effect from ionized dopant. Thus, the ingredient is to keep concentration low and at the same time maintaining high conductivity. As the result of this need, heterojunction modulated doping field effect transistor MODFET is the choice.

The most-common heterojunctions for the MODFETs are formed from AlGaAs/GaAs, AlGaAs/InGaAs, InAlAs/InGaAs, and Al\(_x\)Ga\(_{1-x}\)N/GaN heterojunctions. The better MODFET is fabricated with MBE or MOCVD etc and it is an epitaxial grown heterojunction structures.

Al\(_x\)Ga\(_{1-x}\)As/GaAs MODFET is an unstrained type of heterojunction. This is because the lattice constants of GaAs (5.65 Å) and AlAs (5.66 Å) are almost the same except the energy band-gap. The energy band-gap of gallium arsenide GaAs is 1.42eV, while the energy band-gap of aluminum arsenide AlAs is 2.16eV. The energy band-gap of the alloy can be calculated using equation \(E_G^{\text{Alloy}} = a + bx + Cx^2\), where \(a\), \(b\), and \(c\) are constant for a particular type of alloy. For Al\(_x\)Ga\(_{1-x}\)As, \(a\) is equal to 1.424, \(b\) is equal to 1.247, and \(c\) is equal to 0.

For MODFET fabricated with Al\(_x\)Ga\(_{1-x}\)As/GaAs material, the approach is to create a thin undoped well such as GaAs bounded by wider band-gap modulated doped barrier AlGaAs. The purpose is to suppress impurity...
scattering. When electrons from doped AlGaAs barrier fall into the GaAs, they become trapped electrons. Since the donors are in AlGaAs layer not in intrinsic GaAs layer, there is no impurity scattering in the well. At low temperature the photon scattering due to lattice is much reduced, the mobility is drastically increased. The electron is well is below the donor level of the wide band-gap material. Thus, there is no freeze out problem. This approach is called *modulation doping*. If a MESFET is constructed with the channel along the GaAs well, the advantage would be reduced scattering, high mobility, and no free out problem. Thus, high carrier density can be maintained at low temperature and of course low noise. These features are especially good for deep space reception. This device is called *modulation doped field effect transistor* MODFET and also called *high electron mobility transistor* HEMT or *selective doped* HT. Figure 1.9 illustrates the energy band diagram of $n^+-Al_xGa_{1-x}As$ and $n-$GaAs heterojunction showing $\Delta E_C$ and $\Delta E_G$. The delta energy band-gap between the wide band-gap and narrow energy band-gap device are determined from equation (1.19) and (1.20)

$$\Delta E_C = q(\chi_{\text{narrow}} - \chi_{\text{wide}})$$ (1.19)

and

$$\Delta E_V = \Delta E_G - \Delta E_C$$ (1.20)

$\chi_{\text{wide}}$ and $\chi_{\text{narrow}}$ are respectively the electron affinity of wide band-gap and narrow band-gap semiconductor respectively.

![Figure 1.12: Energy band diagram of $n^+-Al_{0.3}Ga_{0.7}As/n-$GaAs heterojunction](image)
The construction of a recess-gate AlGaAs/GaAs MODFET is shown in Fig. 1.13. The dotted line shows the quantum well where two-dimensional electron gas 2-DEG flows. The undoped AlGaAs, which acts as buffer is 30 – 60 Å thick. The $n$-AlGaAs is around 300 Å thick with concentration of approximately $2 \times 10^{18}$ cm$^{-3}$. For recess-gate type, its thickness is about 500 Å. The source and drain contacts are made of alloy containing germanium such as AuGe. The gate materials can be from titanium Ti, molybdenum Mo, tungsten silicide WSi$_2$, W and Al.

![Figure 1.13: A schematic of a recess-gate $n^+$-Al$_{x}$Ga$_{1-x}$As/GaAs MODFET](image)

### 1.3 Preparation of Facility

In the modern sub-micron integrated circuit fabrication, it requires a multi-million dollar facility that consists of equipment for various fabrication process steps, cleaning stations, and source materials. Beside the equipment, stations, materials are people who are the working in the facility.

The primary quality requirement for the integrated circuit IC facility is cleanliness. The facility is subjected to too many sources of contaminant, which are harmful to device under fabrication. It is the known fact that any contaminant has a size large enough to cover the active area of a sub-micron device. If such type contaminant is resided on the active area of device during fabrication, the consequence is malfunction of the device. Thus, it is necessary for a modern integrated circuit fabrication facility to keep the contaminant and particle levels below part per million ppm or part per billion ppb level.

In modern integrated circuit facility set-up, it employs three-tiered approaches to control the particle level and contaminant level. They are clean facility, wafer cleaning, and gettering. We will describe these approaches in the process of getting clean facility and gettering for integrated circuit fabrication.
1.3.1 Source of Contaminants/Particles

Contaminants/particles are mainly come from people who work in the fabrication facility, equipment in the facility, air circulating in the facility, and the supplied materials from external vendor.

Particle contaminant such as dust particle, particle from cosmetic, powder in the air always present in a distribution of size and shape. However, the most concern size is between 10nm and 10µm. Particle of size 10nm tends to coagulate into a larger size. If the size is larger than 10µm, it will fall by gravity on the surface. Particle of size between 10nm and 10µm remains suspend in air for a long time. Such particle type can be deposited on the surface primary through two mechanisms, which are Brownian motion and gravitational sedimentation. The Brownian motion is a random motion that can occasionally bring the particle and deposit on the surface.

People typically emit 5 to 10 million particles and contaminants per minute from each centimeter square surface. The particle/contaminant emitted by people are mainly from exhaled air, skin, and hair etc, which consist of dust particle, water, salt, carbon dioxide, oxygen, and contaminants such as nickel, manganese, phosphorus etc from powder and cosmetic.

Raw materials such as acid, solvent that brought in from vendor normally contain contaminants after handling even though they are electronic grade materials. The contaminants are required to be filtered out before using.

1.3.2 Clean Facility

Knowing the sources of contaminant, certainly the solution is to eliminate them. If it can be eliminated, it is the best. Otherwise, controlling the amount to the acceptable level is good enough.

A modern sub-micron IC fabrication facility normally is built with class 10 or class 100 cleanliness standards. A class X simply means that each cubic foot of air in the facility has less than X total number of particles of size greater than 0.5µm. In the critical process area such as ion implantation, class 1 cleanliness is required.

Figure 1.14 shows the number of particle versus the diameter of particle expectation for different class of cleanliness for fabrication of the VLSI integrated circuit. Take for an example, the class 100 environment, in one cubic
foot of air, the number of particle of size greater than 0.5μm should not be more than 100.

Figure 1.14: The number of particle and diameter of particle for various classes of cleanliness

Since people working in the integrated circuit fabrication area are continuously emitting contaminant particles which mean this source of contaminant cannot be eliminated. As the result, the particle level in the air will be increased. Thus, the control procedure becomes necessary.

The air in the IC fabrication facility is sucked into the air duct via the vents mounted either on the wall or on the raise floor of the facility. The air is then channel to the ceiling with portion of it is released to the atmosphere, portion of it is mixed with external filter air and is forced through the high efficiency particulate air HEPA filter residing in the ceiling at the velocity of 50cms⁻¹ before it is released into the facility through vent mounted on the ceiling. The release and mixing is necessary to maintain the level of oxygen in the facility.

The HEPA filter is composed of thin porous sheets oftrafine glass fiber of diameter less than 1μm. Large particles having diameter greater than 1μm are trapped by the filter, while the small particles that can pass through will be stuck to the filter due to electrostatic charge. Even if the small particles are not charged, due to work function difference between the particles and filter materials, eventually they are stuck in the filter. The air after filtered by HEPA filter normally has cleanliness better than class 1.
People working in the IC fabrication facility required to wear the “bunny suit” and a pair of clean room shoes, which covers the body and cloth to block the source of contaminant from fabric, human hair, and human sweat. The people are also required to wear face mask to block the particles from the exhaled air getting into the facility. Before entering into the fabrication facility, people have to be cleaned by air shower. Air shower will blow away loose particles/contaminant residing on the cloth and body. Beside all these procedures, people who are working in the fabrication facility are barred from using cosmetic and powder.

Chemical such as sulfuric acid, hydrogen peroxide, acetone, aqueous alkaline, etc used for fabrication process are to be specified as electronic grade types with level of contaminant control to a specific electronic grade standard.

Water is an important solvent for cleaning and rinsing purposes. City water from the tap is too dirty containing too much of contaminants and particles such as chlorine, heavy metals, silt, bacteria etc and is not suitable for cleaning and rinsing. De-ionized DI water is normally used. DI water is the highly purified and filtered water obtained from reverse osmosis process through 0.1nm filter. It has all traces of ionic, particles, and bacterial contaminants been removed.

Another important parameter of DI water is the resistivity. This parameter is important because too low the resistivity value means too much the dissociation of water molecule i.e. too much H⁺ and OH⁻ ions, which would create too much static charge problem on wafer knowing that static charge will attract particles and contaminants.

A basic DI water system can achieve resistivity of 18.0Mohm-cm versus the theoretical resistivity of pure water at temperature 25⁰C, which is 18.3Mohm-cm, with fewer than 1.2 colonies of bacteria per milliliter and no particle size larger than 0.25μm.

1.3.3 Wafer Cleaning

By nature, there is a layer of native oxide grown on silicon wafer due to presence of oxygen in the atmosphere and also due to presence of contaminants such as wax, resin, greasy film, sodium chloride, copper, and etc. Moreover, each process steps, inorganic and organic chemicals such as organic photoresist, hydrochloric acid, developing solution etc are used. The residue of the chemical has to be cleaned before proceeding to next process step. Thus, it is necessary to
clean the wafer before proceed to next fabrication steps. Today there are two types of wafer cleaning technologies namely the wet clean and dry clean technology.

### 1.3.3.1 Wet Cleaning

There are two types cleaning solution for wet cleaning, one for removing organic material and one for removing inorganic material.

Hydrofluoric acid is normally used to remove oxide that formed on surface of silicon wafer. Ammonium hydroxide, sulfuric acid, and hydrogen peroxide are the chemicals typically used to remove organic contaminants, whilst hydrogen peroxide and hydrochloric acid are chemicals used to remove metal/inorganic contaminants. De-ionized DI water is generally used as solvent for cleaning or rinsing. The wafer is finally dried in nitrogen environment and keeps in the storage cabinet with nitrogen circulation to prevent oxidation and contamination.

The right proportional mixture of the above mentioned solvents are termed as Radio Corporation of America RCA solution that was developed in 1965. The solutions are divided into solution clean 1 and solution clean 2. Figure 1.15 shows the eight cleaning steps for cleaning the wafer to remove inorganic, organic, and native oxide contaminants before actual fabrication process steps begin. The figure also shows the composition of various solutions and temperature requirements during cleaning process.

<table>
<thead>
<tr>
<th>Step</th>
<th>Solution</th>
<th>Temperature</th>
<th>Type of Contaminant to be removed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>H₂SO₄ + H₂O₂ (4:1)</td>
<td>120°C</td>
<td>Organic particle</td>
</tr>
<tr>
<td>2</td>
<td>DI water</td>
<td>25°C</td>
<td>Rinse</td>
</tr>
<tr>
<td>3</td>
<td>NH₃OH + H₂O₂ + H₂O (1:1:5)</td>
<td>80°C – 90°C</td>
<td>Organic particle</td>
</tr>
<tr>
<td>4</td>
<td>DI water</td>
<td>25°C</td>
<td>Rinse</td>
</tr>
<tr>
<td>5</td>
<td>HCl + H₂O₂ + H₂O (1:1:6)</td>
<td>80°C – 90°C</td>
<td>Inorganic ion</td>
</tr>
<tr>
<td>6</td>
<td>DI water</td>
<td>25°C</td>
<td>Rinse</td>
</tr>
<tr>
<td>7</td>
<td>HF + H₂O (1:50)</td>
<td>25°C</td>
<td>Native oxide</td>
</tr>
<tr>
<td>8</td>
<td>DI water</td>
<td>25°C</td>
<td>Rinse</td>
</tr>
</tbody>
</table>

![Figure 1.15: Cleaning step and composition of RCA solution](image-url)


1.3.3.2 Dry Cleaning

Wet cleaning method still remains as the major method for wafer cleaning. However, in ULSI microelectronic industry, it has issue related with particle generation, dry difficulty, cost, chemical waste disposal, general flexibility etc. Dry cleaning method provides an alternative for cleaning wafer. Dry cleaning is a gas phase chemistry that requires excitation energy to enhance the chemical reaction at low temperature. The added energy can be plasma, particle beam, short wavelength radiation, or thermal cleaning.

A number of dry cleaning methods have been developed namely HF/H$_2$O vapor cleaning, ultraviolet-ozone cleaning, H$_2$/Ar plasma cleaning, and thermal cleaning. These clean methods are usually used after wet cleaning. Dilute HF acid in wet cleaning usually creates hydrocarbon contamination on the surface of wafer. However, with HF/H$_2$O vapor dry cleaning, the wafer surface is fluorine terminated.

Ultraviolet-ozone cleaning UVOC is an effective way to remove hydrocarbon, although the surface is oxide passivated. The chemical process of UVOC can be explained from equation (1.21) to (1.24). Equation (1.21) is a surface excitation process.

\[
\text{Absorbed impurity} + \text{hv} \rightarrow \text{Excited impurity} \quad (1.21)
\]

In addition, oxygen molecules are excited to UV light to form atomic oxygen. The gas-phase excitation processes are shown in the following equations.

\[
\text{O}_2 + \text{hv} \rightarrow \text{2O} \quad (1.22)
\]

\[
\text{O} + \text{O}_2 \rightarrow \text{O}_3 \quad (1.23)
\]

\[
\text{O}_3 + \text{hv} \rightarrow \text{O} + \text{O}_2 \quad (1.24)
\]

Then the excited impurity like hydrocarbon would react with oxygen atom and ozone to form volatile compound.

Hydrofluoric acid in RCA clean1 and clean 2 solutions promote hydrogen-passivated surface, HF/H$_2$O vapor cleaning induces fluorine terminated surface. When the surface of wafer receiving HF/H$_2$O vapor clean, the content of water
vapor varies with the composition ratios, oxygen content can significantly affect the content of fluorine. Increasing water content can reduce concentration of fluorine.

Ar/H₂ plasma cleaning is used to reduce the bombardment damage to the surface of wafer. Ar and H₂ gas molecules are excited or ionized and will generate plasma with RF of 13.6Mz passing through induction coil at pressure 1.0torr. Excited Ar ion is physically sputtered the surface impurities away, while H₂ ion chemically etch the surface. By proper adjustment of the physical and chemical etching ratio, an optimum cleaning condition can be obtained that produce minimum damaged surface.

1.3.3.3 Thermal Cleaning

The native oxide can be removed by heating the wafer to 800°C or above in ultra high vacuum (< 10^{-10} torr) to vaporize the oxide. The native oxide is SiOₓ, in which x depends on the previous cleaning process. In the Shiraki cleaning process, temperature of 850°C and 10 min duration thermal clean is necessary. However, in the HF dip process with 4% HF, a pre-bake at temperature 200°C is required or no bake process if it is used for a 650°C epitaxial growth.

In all these processes, high temperature cleaning should be carefully examined because at temperature higher than temperature 800°C, the following reaction process occurs at low oxygen partial pressure.

\[
\text{Si} + \text{SiO}_2 \rightarrow 2\text{SiO} \quad (1.25)
\]

The SiO is volatile at temperature above 750°C. When the SiO₂ film is removed, the silicon wafer starts to oxidized following equation (1.26).

\[
\text{Si} + \text{O}_2 \rightarrow \text{SiO}_2 \quad (1.26)
\]

This produces aggravated etching, which induces micro-roughness on the surface. The deposited gate oxide, therefore, has a low breakdown voltage (~1.0MV/cm) due to micro-roughness.

1.3.4 Gettering

Gettering is the third line of control to avoid ionic contaminant reaching the active region of the integrated circuit after facility cleaning and wafer cleaning. The active regions of the integrated circuit usually occupy a small fraction of
the volume of wafer. If there are contaminants resided on them, once they are driven away, the performance of the circuit usually will not be affected because the concentration of contaminant on the active region is now too low to be influential.

Gettering is a process of moving the unwanted contaminant resided in the wafer to the non-critical part of wafer such as the backside of the wafer or far away from the active parts on the top of wafer. The contaminants that are the most concern which requiring gettering, are heavy transition elements such as titanium, chromium, mercury, copper etc. They are normally the deep level contaminants found in silicon wafer due to high diffusion coefficient. The other most concern contaminants are alkali ions such as sodium Na\(^+\) and potassium K\(^+\) that usually come from human sweat commonly residing in dielectric material that can cause threshold shift of the MOSFET.

The processes of gettering consist of three steps. Firstly, the elements to be gettered must be freed from any trapping sites that they are currently occupied and made mobile. Secondly, they must diffuse to the gettering site and finally, they must be trapped permanently.

1.3.4.1 Alkali Gettering

Phosphosilicate glass PSG containing 5% by weight of phosphorus, is normally deposited on top of the wafer to prevent contamination. It is a good material that can drive alkali ions from contaminating the dielectric material or draw alkali contaminant from dielectric material. PSG that has chemical name \(\text{P}_2\text{O}_5/\text{SiO}_2\), is normally deposited using chemical vapor deposition CVD or low pressure chemical vapor deposition LPCVD covering the top of the wafer. It traps alkali ions and forms a stable compound that binds sodium Na\(^+\) and potassium K\(^+\) ions. Thus, it is an effective way to prevent these ions diffusing into the dielectric region or drawing these ions from dielectric materials.

The shortcoming of PSG is its charge dipole nature. After trapping ions, it can affect the surface electric field. Moreover, it is susceptible to absorbing water vapor that can cause aluminum corrosion. These effects can be minimized by controlling the percentage of phosphorus content. In the case of MOSFET fabrication, silicon nitride \(\text{Si}_3\text{N}_4\) is used to prevent this problem. This layer is impermeable to alkali ions and can form effective barrier to diffusion.
1.3.4.2 Heavy Metal Gettering

Heavy metallic elements such as copper, nickel etc have two basic properties. These elements have high diffusion coefficient. Thus, they are normally deeply trapped in the silicon wafer. The second property is that atoms of these elements have preferential residing site in the crystal lattice where imperfection exist. Thus, one can see that the principle of gettering contamination of heavy metal is to create imperfection site in the crystal lattice or trapping center.

There are two basic gettering methods to draw away heavy metallic element, which are extrinsic and intrinsic getterings. The extrinsic gettering makes used of the backside of the wafer explicitly creating trapped center to trap such contaminant. Intrinsic gettering makes use of the properties of Czochralski CZ silicon that contains oxygen to precipitate and trap metallic contaminants because oxygen is a recombination center. Note that during the Czochralski silicon ingot growth process, the molten silicon etches or dissolves the quartz crucible wall to generate oxygen.

Intrinsic gettering uses the oxygen content in CZ silicon, which is normally at the substrate region of the silicon wafer distanced away from the epitaxial layer which is part of the device region. The concentration of oxygen in the CZ silicon is normally in 10 to 20ppm, which is about $10^{18}$cm$^{-3}$. Oxygen can react with silicon to form silicon dioxide SiO$_2$ due to high process temperature. Owing to the difference in size of SiO$_2$ and silicon atom, stack fault is normally occurred which means dislocation or imperfection exist for precipitation or trap site for the heavy metallic contaminant. One may ask why precipitation does not occur in epitaxial layer. The answer is that the epitaxial layer is a fabrication process that it has much lower oxygen content and is not sufficient enough for precipitation.

1.4 Crystal Growth
Before the fabrication of the integrated circuit, the preparation of silicon or gallium arsenide wafer is required. The preparation of wafer involves several process steps. They are distillation and reduction/synthesis, crystal growth, grind/saw/polish, and electrical and mechanical characterizations. We shall not discuss the process of making gallium arsenide GaAs wafer. We shall concentrate on the process of making silicon wafer.

The starting material is silicon dioxide for making silicon wafer. It is chemically processed to form a high-purity crystal polycrystalline semiconductor for which single crystal is formed. The single crystal ingot is shaped to defined diameter and is sawed into wafer. The wafer is then etched and polished to provide smooth, specular surface where device is fabricated.

Pure form of sand SiO₂ called quartzile is placed in high temperature furnace with various forms of carbon like coke, coal, and even wood chip. Owing to silicon dioxide is very stable, carbon is used to replace silicon to form carbon dioxide at reduce temperature. There are numbers of reaction are taken place. Nevertheless the overall reactions follow equation (1.27).

\[
\text{SiO}_2 + 2\text{C} \rightarrow \text{Si} + 2\text{CO}↑ \quad (1.27)
\]

This process generates polycrystalline silicon with about 98% to 99% purity, which is called crude silicon or metallurgical-grade silicon MGS.

The next process step is silicon purification step. Silicon is pulverized and treated with hydrochloric acid gas HCl at temperature 300°C to form trichlorosilane SiHCl₃ vapor. The chemical reaction follows equation (1.28).

\[
\text{Si} + 3\text{HCl} \xrightarrow{300°C} \text{SiHCl}_3 + \text{H}_2↑ \quad (1.28)
\]

Trichlorosilane TCS vapor is then gone to fractional distillation to remove unwanted impurities through a series of filters, condensers (boiling point 32°C), and purifiers to finally get an ultra high purity liquid of purity higher than 99.99999999% at room temperature. The high-purity TCS is then used in the hydrogen reduction reaction at temperature 1,100°C to produce the electronic grade silicon EGS.

\[
\text{SiHCl}_3 + \text{H}_2 \xrightarrow{1,100°C} \text{Si} + 3\text{HCl}↑ \quad (1.29)
\]

The reaction takes place in a reactor containing resistance heated silicon rod, which serves as the nucleation point for deposition of EGS in polycrystalline
form of high purity. This is the raw material used to prepare device quality single crystal. Pure EGS has impurity concentration generally in part per billion. The pure EGS is then ready to be pulled into silicon ingot for making wafer that used to fabricate integrated circuit.

There are a number of methods used to grow silicon crystalline ingot. We shall discuss three methods here namely Czochralski, Float-zone methods, and Bridgman-Stockbarger technique. There are other methods such as liquid encapsulated Czochralski LEC, micro-pulling-down μ-PD, laser-heated pedestal growth LHPG or laser floating zone LFZ etc are not discussed here.

1.4.1 Czochralski Crystal Growth Method

Czochralski crystal growth method was invented by a polish chemist named Jan Czochralski. The polycrystalline silicon is melt at temperature 1,415°C just above the melting point temperature of silicon, which is 1,414°C, in the argon Ar atmosphere in quartz crucible by radio frequency RF or resistive heating coil. Right type and the amount of dopant are then added. With the aid of “seed”, silicon rod of right diameter is formed by rotation and pulling in Czochralski CZ puller as shown in Fig. 1.16. Figure 1.16(a) shows the photograph of a modern computer-controlled Czochralski crystal puller. Figure 1.16(b) is the schematic drawing showing the components of the puller.

Once thermal equilibrium is established, the temperature at the vicinity of the seed is reduced and the molten silicon begins to freeze out onto the seed crystal. Subsequently, the seed is slowly rotated and withdrawn at the rate of a few millimeter per minute to form a cylindrically shaped single crystal of silicon, which is known as ingot.

The diameter of the crystal in CZ method can be controlled by temperature and pulling rate using automatic diameter control system. Typically, 4 to 6 inch diameter and 1 to 2 meter in length type of ingot can be formed. In today’s process, ingot of diameter as large as 12 inches is commonly produced to save cost and improve productivity. However, for large ingot as large as 12 inches in diameter, an external magnetic field is applied around the crucible and it is used to control the concentration of defects, impurities, and oxygen.

18 inches wafer is currently under studied and it is expected to turn out first wafer in 2018.
1.4.1.1 Impurity of Czochralski Process

The crystal ingot growth by Czochralski method always has trace impurities of oxygen and carbon, which come from silica and graphite crucible materials. Silica is silicon dioxide, which is the source of oxygen. Silica will react with graphite to form carbon monoxide, which is the source of carbon. The equation of chemical reaction is shown in equation (1.28).

\[
\text{SiO}_2 + 3\text{C} \rightarrow \text{SiC} + 2\text{CO} \tag{1.28}
\]

Typically, the oxygen concentration is approximately ranged from \(1.0 \times 10^{16}\text{ cm}^{-3}\) to \(1.5 \times 10^{18}\text{ cm}^{-3}\) and the concentration of carbon varies from \(2.0 \times 10^{16}\text{ cm}^{-3}\) to \(1.0 \times 10^{17}\text{ cm}^{-3}\). The contents of oxygen and carbon are very much depending on ambient pressure, pulling and rotation rate, and the ratio of the diameter and the length of the ingot.
1.4.1.2 Concentration of Czochralski Process

In the crystal growth process, the most common dopants is boron and phosphorus, which are used to make $p$- and $n$-type semiconductor materials respectively. As the crystal is pulled from the molten silicon, the doping concentration incorporated into the crystal is usually different from the doping concentration of the molten silicon at the interface. The ratio of these two concentrations is *equilibrium segregation coefficient* $k_0$, which is defined as

$$k_0 = \frac{C_s}{C_I}$$

(1.31)

where $C_s$ and $C_I$ are respectively the equilibrium concentration of the dopant in the solid and liquid near interface. Figure 1.17 shows the equilibrium segregation coefficient of the common dopants used for silicon. The value below one means that during the growth the dopants are rejected into the molten silicon. As the result, the dopant concentration of molten silicon becomes higher as time lapsed.

<table>
<thead>
<tr>
<th>Dopant</th>
<th>$k_0$</th>
<th>Type</th>
<th>Dopant</th>
<th>$k_0$</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>8.0x10^-1</td>
<td>$p$</td>
<td>As</td>
<td>3.0x10^-1</td>
<td>$n$</td>
</tr>
<tr>
<td>Al</td>
<td>3.0x10^-3</td>
<td>$p$</td>
<td>Sb</td>
<td>3.3x10^-2</td>
<td>$n$</td>
</tr>
<tr>
<td>Ga</td>
<td>8.0x10^-3</td>
<td>$p$</td>
<td>Te</td>
<td>3.0x10^-4</td>
<td>$n$</td>
</tr>
<tr>
<td>In</td>
<td>4.0x10^-4</td>
<td>$p$</td>
<td>Li</td>
<td>1.0x10^-2</td>
<td>Deep-lying impurity level</td>
</tr>
<tr>
<td>O</td>
<td>1.25</td>
<td>$n$</td>
<td>Cu</td>
<td>4.0x10^-1</td>
<td>Deep-lying impurity level</td>
</tr>
<tr>
<td>C</td>
<td>7.0x10^-2</td>
<td>$n$</td>
<td>Au</td>
<td>5.0x10^-5</td>
<td>Deep-lying impurity level</td>
</tr>
<tr>
<td>P</td>
<td>0.35</td>
<td>$n$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 1.17: Equilibrium segregation coefficients for dopant in silicon

Let’s consider a crystal being growth from the initial molten silicon of weight $M_o$ with an initial doping concentration $C_o$ (the weight of dopant per 1g of molten silicon) in the molten silicon. At a given time, a crystal of weight $M$ has been grown, the amount of the dopant remaining in the molten silicon by weight is $S$. For an incremental amount of the crystal with weight $dM$, the
corresponding reduction of the dopant -dS from the molten is $C_S dM$, where $C_S$ is the doping concentration in the crystal by weight.

$$-dS = C_S dM$$

(1.32)

The remaining weight of the molten silicon is $(M_0 - M)$ and the doping concentration in liquid by weight $C_1$ is given by

$$C_1 = \frac{S}{M_0 - M}$$

(1.33)

Substituting equation (1.32) and (1.33) into equation (1.31), it yields equation (1.28).

$$\frac{dS}{S} = -k_0 \left( \frac{dM}{M_0 - M} \right)$$

(1.34)

Given that the initial weight of the dopant is $C_o M_0$, integration equation (1.34) yields equation (1.35).

$$\int_{C,M_0}^{C,S} \frac{dS}{S} = -k_0 \int_0^M \frac{dM}{M_0 - M}$$

(1.35)

Solving equation (1.35) and combining with equation (1.33), it yields equation (1.36).

$$C_S = k_o C_o \left( 1 - \frac{M}{M_0} \right)^{k_0 - 1}$$

(1.36)

During the growth of silicon ingot, dopant is constantly being rejected into the molten silicon. If the rejection rate is higher than the rate at which the dopant can be transported away by diffusion or stirring, then a concentration gradient will develop at the interface as shown in Fig. 1.18. The equilibrium segregation coefficient is equal to $k_0 = C_S/C_1(0)$. We can define an effective segregation coefficient $k_e$, which is the ratio of $C_S$ and the impurity concentration far away from the interface.

$$k_e \equiv \frac{C_S}{C_1}$$

(1.37)
Let’s consider a small virtual stagnant molten layer of width $\delta$ in which the only flow that required to replace the crystal being withdrawn from the molten. Outside the stagnant layer the concentration remains constant at $C_1$. In the layer, the concentration can be described by steady state continuation equation.

$$D \frac{d^2C}{dx^2} + v \frac{dC}{dx} = 0$$ (1.38)

where $D$ is the diffusion coefficient of the molten silicon and $v$ is the velocity of the crystal growth. The solution of equation is $C = A_1 e^{-vx/D} + A_2$ with the constant to be determined by two boundary conditions. The first is at $x = 0$, $C = C_I(0)$ and second is determined by conservation of total number of dopant i.e. the sum of dopant flux at interface is zero. This condition yields equation.

$$D \left( \frac{dC}{dx} \right)_{x=0} + [C_I(0) + C_S] = 0$$ (1.39)

Substituting the conditions and $C = C_I$ at $x = \delta$, the solution for the concentration $C$ is

$$e^{-\delta v/D} = \frac{C_I - C_S}{C_I(0) - C_S}$$ (1.40)

The effective segregation coefficient $k_e$
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\[ k_e = \frac{C_s}{C_i} = \frac{k_0}{k_0 + (1-k_0)e^{-v/\delta/D}} \]  \hspace{1cm} (1.41)

1.4.1.3 Pull Rate of Czochralski Process

Pertaining pull rate of Czochralski crystal growth, one expects the pull rate should be slower for larger diameter ingot. Indeed the pull rate is inversely proportional to the square root of diameter of ingot. It can be derived based on the first order heat balance equation, which represents the dominant heat fluxes present during freezing process. Reference to Fig. 1.19, \( x_1 \) is a constant temperature surface, which is isotherm just inside the liquid. \( x_2 \) is an isotherm just inside the solid. During freezing process, which occurs between these isotherms, heat is released to allow the silicon to transform from liquid to solid state, which is heat of fusion. This heat must be removed from freezing interface. It is a primary process of heat transfer by conduction up to the solid ingot. Thus, one can write equation (1.42).

\[ L \frac{dm}{dt} + k_L \frac{dT}{dx_1} A_1 = k_s \frac{dT}{dx_2} A_2 \]  \hspace{1cm} (1.42)

where \( L \) is the latent heat of fusion, \( dm/dt \) is the amount of silicon freezing per unit time, \( k_L \) is the thermal conductivity of liquid, \( dT/dx_1 \) is the temperature gradient across the isotherm \( x_1 \), \( k_s \) is the thermal conductivity of the solid. \( dT/dx_2 \) is the temperature gradient across the isotherm \( x_2 \), and \( A_1 \) and \( A_2 \) are respectively the cross sectional areas.

Figure 1.19: Freezing process occurring during Czochralski crystal growth
The middle term of equation (1.42) will drop from this point onward, which is representing any additional heat may flow from the liquid to the solid because of the temperature gradient between the two. By neglecting it, one can include only the absolute minimum heat which must be transported away from the freezing interface. The effect on the final result will be that the pull rate will be the maximum. If area $A_1$ and $A_2$ is equal to $A$ then the rate of crystal $V_p$ is pulled out of the molten silicon is simply equal to

$$\frac{dm}{dt} = V_pAN$$  \hspace{1cm} (1.43)

Substituting equation (1.43) into equation (1.42) after ignoring the middle term of the equation, it becomes

$$V_{p,\text{MAX}} = \frac{k_s}{LN} \frac{dT}{dx}$$  \hspace{1cm} (1.44)

$V_{p,\text{MAX}}$ is the maximum pull rate and $N$ is the density of silicon.

In order to eliminate the temperature gradient term from equation (1.44), one needs to consider how the heat is conducted up the solid crystal and how it is eliminated from the solid ingot. Reference to Fig. 1.19, the latent heat of crystallization (A) is transferred from molten silicon to solid ingot. The heat is then transported away from the freezing interface primarily by conduction up the solid ingot (B). The heat is lost from ingot by radiation (C) and by convection, although one will consider only radiation to keep the analysis simple.

The Stefan-Boltzmann law describes heat loss due to radiation (C) is

$$dQ = (2\pi rd)(\sigma \varepsilon T^\frac{4}{3})$$  \hspace{1cm} (1.45)

where $2\pi rdx$ represents the radiating surface area of an increment length of the ingot. $\sigma$ is Stefan-Boltzmann constant and $\varepsilon$ is the emissivity of the silicon.

The heat conducted up the ingot (B) is given by

$$Q = k_s(\pi r^2)\frac{dT}{dx}$$  \hspace{1cm} (1.46)
where the $\pi r^2$ term is the cross sectional area of the ingot conducting the heat and $dT/dx$ is the temperature gradient. Differentiating equation (1.46) yields

$$\frac{dQ}{dx} = k_s(\pi r^2) \frac{d^2T}{dx^2} + (\pi r^2) \frac{dT}{dx} \cdot \frac{dk_s}{dx} \approx k_s(\pi r^2) \frac{d^2T}{dx^2}$$

(1.47)

The second term in the derivative is normally neglected in comparison to the first term. Substituting equation (1.47) into equation (1.45), it yields equation (1.46).

$$\frac{d^2T}{dx^2} - \frac{2\sigma \varepsilon}{k_s} T^4 = 0$$

(1.48)

This equation describes the temperature profile up to the solid ingot. The thermal conductivity of solid $k_s$ varies approximately inverse of temperature i.e. $1/T$ at least for temperature below about $1,000^\circ C$. Thus, the conductivity of solid $k_s$ is

$$k_s = k_M \frac{T_M}{T}$$

(1.49)

where $k_M$ is the thermal conductivity at the melting temperature $T_M$. Thus equation (1.48) becomes equation (1.48) after substituting equation (1.49).

$$\frac{d^2T}{dx^2} - \frac{2\sigma \varepsilon}{k_M T_M} T^4 = 0$$

(1.50)

This differential equation has solution, which is

$$T = \left( \frac{3k_M T_M}{8\sigma \varepsilon} \right)^{\frac{1}{3}} \frac{1}{\sqrt{x + \left( \frac{3k_M r}{8\sigma \varepsilon T_M^3} \right)^{\frac{1}{2}}}}$$

(1.51)

Differentiating equation (1.51) with respect to $x$ and evaluating the result for $x = 0$, which at freezing interface and substituting the result into equation (1.44), the maximum pull rate of the ingot is

$$V_{p\text{MAX}} = \frac{1}{\text{LN}} \sqrt{\frac{2\sigma \varepsilon k_M T_M^5}{3r}}$$

(1.52)
Equation (1.52) has clearly shown that the maximum pull rate $V_{pMAX}$ is proportional to square root of the ingot’s radius.

### 1.4.2 Float-Zone Crystal Growth Method

The method is discovered by William Gardner Pfann. The float-zone crystal growth method is illustrated conceptually in Fig. 1.20. The crystal is not grown in the crucible that it has markedly reduced the impurity level particularly the level of oxygen and carbon. It is grown in sealed furnace with argon Ar gas. This method is used today for fabricating device that requires high resistivity and low oxygen content in the power device and detector device.

In the float-zone process, a polysilicon rod of EGS is clamped at both ends, with bottom in contact with a single-crystal seed. A small RF coil provides large current in silicon that locally melts the silicon. The molten zone is usually 2.0cm long. The liquid phase silicon is then bonded to the atomic plane of the seed plane by plane as the zone is slowly moved up. Doping of the crystal can be achieved by either starting with a doped polysilicon rod, a doped seed, or maintaining a gas ambient during the process that contains a dilute concentration of the desired dopant.

![Figure 1.20: Basic float-zone crystal growth method](image_url)
Segregation effect also plays an important role in the float-zone process just as it did in Czochralski method. It is illustrated from derivation of concentration of solid silicon $C_s(x)$ formed as it moves from molten state at the bottom to the top.

Figure 1.21 shows the idealized geometry of zone length $L$. The rod has initial concentration of $C_0$.

If the molten zone moves upwards by a distance $dx$, the number of impurities in the liquid zone will change since some will dissolve into the melting liquid at the top and some will be lost to the freezing solid at the bottom. Thus,

$$dI = (C_0 - k_0 C_I) dx$$

where $I$ is the number of impurities in the liquid. However, concentration of molten silicon is $C_I = I/L$. Thus, substituting it into equation (1.53) and integrating, it yields equation (1.54).

$$\int_0^x dx = \int \frac{dI}{k_0 C_0 - \frac{k_0 I}{L}}$$

where $I_0$ is the number of impurities in the zone when it is first formed at the bottom. Performing the integration and noting that $I_0 = C_0/L$ and $C_s = k_0 I/L$, the concentration of solid $C_s(x)$ at distance $x$ is

$$C_s(x) = C_0 \left[ 1 - (1 - k_0) e^{-\frac{k_0 x}{L}} \right]$$

As compared to Czochralski method, float-zone method has a greater resistivity variation. Thus, Czochralski method is still the dominant method for large diameter silicon crystal. The melt-crystal interface is very complex for float-zone method, so it is difficult to get dislocation free crystal. Unlike Czochralski method, it needs a high-purity polysilicon to begin.
1.4.3 Bridgman-Stockbarger Crystal Growth Method

The set-up of Bridgman-Stockbarger crystal growth technique is shown in Fig. 1.22. This method is named after Harvard physicist Percy Williams Bridgman and MIT physicist Donald C. Stockbarger. The molten silicon or germanium is placed in crucible. With a small crystal placed at one end. The crucible is pulled slowly in the horizontal direction. As the molten zone moves out of the furnace, it is slowly cooled and silicon or germanium solidifies following the crystal.

1.5 Wafer Process

After the growth of silicon ingot, the ingot is machined cut at the end and polishes the sides to remove grooves created by automatic diameter control
system. The flat of 150mm or smaller, or notch of 200mm or larger is grinded on the ingot to mark the crystal orientation.

The ingot is then sliced into wafer thickness of about 150µm depending on the diameter of the wafer using a rapid-rotating inward-diameter diamond-coated saw. After sawing, the wafer is grinded to round shaped edge to prevent edge chipping during mechanical handling of wafer processing.

The wafer is then rough polished by conventional abrasive, glycerin slurry with fine alumina Al₂O₃ suspension-lapping process to remove the majority of surface damage. It is necessary to create a flat surface for photolithography. The process can produce surface flatness within 2.0µm. During the lapping process, about 50µm of silicon is removed from both side of 150µm wafer.

After lapping process, a wet etch process is necessary to remove remaining damage that can be as deep as 10µm into the silicon. Thus, wet etch would remove 10µm from both sides of the wafer. The wet etchant is a mixture of nitric acid HNO₃, hydrofluoric acid HF, and acetic acid CH₃COOH. Nitric acid reacts with silicon to form silicon dioxide, while hydrofluoric acid then removes the oxide. Acetic acid is used to control the rate of reaction. The wet process further smoothen the surface due to isotropic etch characteristics with nitric acid-rich solution. The usual formation is a 4:1:3 mixture of nitric acid (79wt% in H₂O), HF (49wt% in H₂O), and pure acetic acid. The chemical reaction equation for the wet etch process is expressed in equation (1.56).

\[3Si + 4HNO_3 + 6HF \rightarrow 3H_2SiF_6 + 8H_2O + 4NO↑\]  \hspace{1cm} (1.56)

The last process is chemical mechanical polishing CMP as shown in Fig. 1.23. Chemical mechanical polishing process has been used to prepare silicon Si wafers for more than 30 years, as well as for glass polishing and for bonded silicon-on-insulator SOI wafers. Although its application to interlayer dielectric ILD planarization is more recent, both the equipment and the technique are well known to the semiconductor industry. The wafer is held on a rotating holder and pressed on a rotating polishing pad with slurry and water in between. The slurry is a colloidal suspension of fine silica SiO₂ particle with diameter of about 100Å in an aqueous solution of sodium hydroxide. Sodium hydroxide oxidizes, which is a chemical process, the silicon surface with the help of heat generated by friction between wafer and polishing pad. The silica particle then abrades the silicon dioxide away from the surface – a mechanical process.
The basic polishing mechanism for silicon dioxide \( \text{SiO}_2 \) dielectric is the same as for glass polishing. The mechanical removal rate \( R \) of the glass is given by the Preston equation.

\[
R = K_p p v
\]  

(1.57)

where \( R \) is rate of removal; \( p \) is applied pressure; \( v \) is relative velocity between the wafer and the polishing pad; and \( K_p \) is the proportionality, whereby it has units of \((\text{pressure})^{-1}\) and is also known as the Preston coefficient. \( K_p \) is a function of the mechanical properties of the glass (hardness, Young’s modulus), the polishing, slurry, and the composition and the structure of the polishing pads.

The post CPM process is a cleaning process with a mixture of acid-oxidizer solution to remove organic and inorganic contaminant and particles (RCA clean 1 and clean 2 solutions). Dry cleaning also can be applied in cleaning process. The finished wafer has a defect-free surface.

The finished processed wafer has to undergo sample electrical and mechanical properties measurement before it is finally released to IC fabrication facility. The electrical test includes mobility, resistivity, doping concentration etc.

At the back of wafer, defect and dislocation are intentionally created to trap heavy metal, mobile, oxygen, carbon, and other alkaline contaminant as
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mentioned in earlier Section. Back side defect can also be created using argon ion implantation, polysilicon deposition, and heavily doped phosphorus. During fabrication, the backside of the wafer is usually always deposited with a chemical vapor deposition CVD silicon dioxide or silicon nitride Si$_3$N$_4$ layer to prevent any out diffusion during thermal process.

**Exercises**

1.1. Name two factors that make silicon the most attractive semiconductor material in electronic application.

1.2. Name three properties and applications of wide band-gap semiconductor materials.

1.3. Explain why the conductivity of the intrinsic semiconductor is low at room temperature.

1.4. A silicon step junction at temperature 300K equilibrium condition has a $p$-side doping with $N_A = 2 \times 10^{15}$ cm$^3$ and $n$-side doping with $N_D = 1 \times 10^{17}$ cm$^3$. Calculate the built-in potential $V_{bi}$.

1.5. Determine all carrier concentrations in a Si $p^+n$ junction and given that the slope of $1/C^2$ versus $V_R$ graph is $1.32 \times 10^{14}$ F cm$^{-2}$ V$^{-1}$ and built-in potential $V_{bi}$ is 0.850V.

1.6. Discuss conceptually how an $npn$ Si bipolar junction transistor shall be designed?

1.7. What are carrier components in an $npn$ Si bipolar junction transistor when it is biased in forward active mode?

1.8. Define the emitter efficiency $\gamma_e$ for a BJT. Discuss how you can improve the emitter efficiency for a bipolar junction transistor.

1.7. Consider an $n$-channel MOSFET with gate width $W = 10\mu$m and gate length $L = 1.5\mu$m and oxide capacitance $C_{ox} = 10^{-7}$ F/cm$^2$. In the linear region for a fixed $V_{DS} = 0.1$V, the drain current is found to be 40$\mu$A for $V_{GS} = 1.5$V and 80$\mu$A for $V_{GS} = 2.5$V. Calculate the threshold voltage $V_t$ and mobility $\mu_n$ of this MOSFET. Comment the obtained value of mobility.

1.8. Name two advantages of GaAs technologies over CMOS technologies.
A GaAs MESFET with gold Schottky barrier of barrier height 0.8V has $n$-channel doing concentration $2.0 \times 10^{17} \text{cm}^{-3}$ and channel thickness 0.25$\mu$m. Calculate the threshold voltage for this MESFET.

The energy band diagram of $n^+\text{-Al}_{0.3}\text{Ga}_{0.7}\text{As}/n\text{-GaAs}$ heterojunction is shown in the figure. Calculate the delta energy band-gap and electron affinity of Al$_{0.3}$Ga$_{0.7}$As.

Name three-tiered approaches used to control the particle level and contaminant level in fabrication facility.

Describe how gettering of heavy metal can be achieved.

Describe how the high efficiency particulate air filter can filter the air inlet to the fabrication facility to class-one cleanliness.

State the reason why DI wafer is used for wafer rinsing.

Given a silicon wafer to you, how do you identify its crystal orientation and the type of dopant it contains?

Name two methods that can be used to getter away heavy alkaline ion contaminant from the integrated circuit.

State the disadvantage of phosphosilicate glass for gettering the alkaline contaminant.
1.17. The seed crystal used in the Czochralski process is usually necked down to a small diameter of 5.5mm as a means to initiate dislocation-free growth. If the critical yield strength of silicon is $2.0 \times 10^6 \text{ g/cm}^2$, calculate the maximum length of a silicon ingot 200mm in diameter that can be supported by such a seed. Given the density of the silicon ingot is 2.33g/cm$^3$.

1.18. A silicon ingot contains $2.0 \times 10^{18}$ phosphorus atoms cm$^{-3}$ is to be grown by the Czochralski technique. Given that the density of molten silicon is 2.53g/cm$^3$, the atomic weight of phosphorus is 30.97g, and the segregation coefficient of phosphorus is 0.35.

(i) What is the concentration of phosphorus atoms should be in the molten silicon to give the required concentration in ingot?

(ii) If the initial load of silicon in crucible is 150.0kg, how many grams of phosphorus should be added?

1.19. A silicon ingot contains $10^{16}$ boron atoms cm$^{-3}$ is to be grown by the Czochralski technique. The initial load of silicon in crucible is 60kg. After 60% of the molten silicon has been converted into solid silicon, what is the amount of solid silicon required to be added to the molten silicon so that it can get back its initial concentration? Given the density of molten silicon is 2.53g/cm$^3$. 

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