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Chapter 11

Low Power VLSI Circuits

11.0 Introduction

In this Chapter the ways that the power dissipation of the logic circuit is derived, which consist of static and dynamic power. The components of the static and dynamic power are studied in details. The Chapter tells us how to identify the physical aspect of device design and layout of the integrated circuit in attempt to find the causes of the power dissipation. After identifying the causes, the methods used to reduce power dissipation of the logic circuit, which is a demanding need in today’s portable devices requirements for low power dissipation and prolonging the operating time of the battery, are studied. The methods include multiply supply power approach, reducing dimension of the device, using concept of parallel/pipeline operation, variable threshold approach etc. In the final part of the Chapter, the actual logic circuits using adiabatic circuit design for power dissipation reduction is studied.

11.1 Power Consumption Analysis

Unlike bipolar circuit, circuit design with CMOS transistor consumed least amount power when it is in static mode. This is because the $p$-MOS and $n$-MOS transistor networks of the CMOS circuit are connected in series. Thus, theoretically CMOS should not consume any power while it is in static mode. In actual scenario, it does consume power. The dimension of MOS transistor is much small than bipolar transistor, dynamic power consumption of the MOS transistor consumes much smaller power than bipolar transistor. In the normal circumstances, MOS transistor circuit requires low power rail source. Thus, it is another contributor of low power consumption. With the mentioned advantages and the design method, circuits designed with CMOS technology has long been an ideal design for portable device that required a small battery to power the device for several hours.

In this Section, we will learn how to use CMOS transistor to design circuit that has least power consumption. The methods used to derive the static and dynamic power equation for a simple CMOS logic gate are studied. At the end
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of this sub-section, the analysis the power consumption of a complex logic circuit is studied.

11.1.1 Static and Dynamic Power of CMOS Logic Circuit

We from earlier Chapter 5 that CMOS circuit is consists of a $p$-MOS network circuit connected parallel with an $n$-MOS transistor network. Since the circuit is operated in complimentary mode, which means that there is no one instant of time that any one of the $p$-MOS transistor of the $p$-MOS transistor network and any none of the $n$-MOS transistor of the $n$-MOS transistor that are connected in series are switched on simultaneously. Thus, theoretically the circuit should not consume any dynamic power when they are static mode. The illustration of the circuit showing no simultaneously switching of the $p$-MOS and $n$-MOS series connected transistors is shown in Fig. 11.1.

![Figure 11.1: Logic circuit in switching mode showing no $n$-MOS and $p$-MOS transistors series connected is switched on simultaneously. Note: red colour indicates logic 1 and white colour indicates logic 0](image)

Although the CMOS circuit is in static mode, there is static power consumed due to the reasons described here in the text. The static power dissipation of CMOS circuits is primary caused by mainly three sources namely the leaking current, which determined by fabrication technology, consist of reverse bias current in the parasitic diodes formed between source/drain diffusion region and the bulk region in the MOS transistor structure as well as the sub-threshold
current that arises from the inversion charge that exits at the gate voltages below the threshold voltage, and tunneling current through the gate oxide to the drain. The above described sources of power dissipation of the CMOS circuit are termed as static power $P_{\text{DC}}$.

Another source of power dissipation is dynamic power $P_{\text{dyn}}$. Dynamic power comes from mainly three sources. Short-circuit current is one of them, which is due to the dc path between the supply voltage $V_{\text{DD}}$ and the ground rail $V_{\text{SS}}$ during the output transitions. This happens when both the $p$-MOS transistor and $n$-MOS transistor are in saturation mode. The second contribution of the power dissipation is charging and discharging of the capacitive load $C_{\text{out}}$ during the logic changes at the output. The third contribution is coming from glitching power caused by gate delay.

### 11.1.2 Static Power Dissipation

Sub-threshold current is one of the non-ideal effects of MOS-transistor which has been studied. When the MOS transistor is in the switch-off mode, in which the gate-to-source voltage is lower than its threshold voltage, the current flow between the drain and source is not abruptly equal to zero. The sub-threshold current $I_{\text{DS-Sub}}$ drop exponentially following equation (11.1), an equation for $n$-MOS transistor.

$$I_{\text{DS-Sub}} = \mu_n C_{\text{ox}} \frac{W}{L} \left(\frac{kT}{q}\right)^2 \exp\left[\frac{q(V_{\text{GS}} - V_t)}{\eta kT}\right] \left[1 - \exp\left(-\frac{qV_{\text{DS}}}{kT}\right)\right]$$  \hspace{1cm} (11.1)

where $\mu_n$ is the electron mobility, $C_{\text{ox}}$ is the gate capacitance per unit area, $W$ is the channel width, $L$ is the channel length, $V_t$ is the threshold voltage of the MOS, and $\eta$ is the sub-threshold parameter related to the sub-threshold swing $S$, which is the gate voltage change needed to raise the sub-threshold current by one decade following the equation $S = \eta V_t (\ln 10)$. The sub-threshold parameter $\eta$ is given by

$$\eta = 1 + \frac{C_D}{C_{\text{ox}}}$$  \hspace{1cm} (11.2)

where $C_D$ is the depletion channel capacitance per unit area.
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Sub-threshold conduction is exacerbated by drain-induced barrier lowering (DIBL) – another non-ideal parameter of MOS transistor, in which the positive drain-to-source voltage \( V_{DS} \) effectively reduce the threshold voltage \( V_t \).

Junction leakage \( I_{\text{Leak}} \) between drain/source and bulk follows the reverse bias diode current-voltage equation, which is

\[
I_{\text{Leak}} = I_S \left( e^{V_D/V_T} - 1 \right) \tag{11.3}
\]

where \( I_S \) is the reverse saturation current, \( V_D \) is the reverse bias voltage applied to the junction, and \( V_T \) is the thermal voltage. Note that reverse saturation current is temperature, doping concentration, and diffusion coefficient dependent. Thermal voltage is also temperature dependent, which follows equation \( V_T = K T / q \), where \( K \) is Boltzmann constant. There are other forms of leakage such as tunneling current, in which according to quantum mechanics, there is finite probability that carrier will tunnel through the gate oxide. This results in gate leakage current flowing into gate.

For a logic gate, the static power dissipation is equal to

\[
P_{DC} = V_{DD} I_{\text{DDQ}} \tag{11.4}
\]

where \( I_{\text{DDQ}} \) is the measured static current or quiescent leakage current.

11.1.3 Dynamic Power Dissipation

Based on the voltage characteristic curve VTC that has been studied in Chapter 10, the drain current consumption plot during the output transition of NOT gate is shown in Fig. 11.2. One has to take note that during the transition of the output voltage either changing from logic 1 to logic 0 or from logic 0 to logic 1, the maximum dc current consumption occurred when output voltage is equal to input voltage, which is the mid-point voltage \( V_M \) illustrated in Fig. 11.2 at point 3. At this point, both \( p \)-MOS and \( n \)-MOS transistors are in saturation mode. It is obvious to say the maximum current drain occurred when the both \( n \)-MOS and \( p \)-MOS transistors are connected in series are in saturation mode. The current is also termed as instantaneous short current because the supply voltage \( V_{DD} \) is connected to ground via the series small channel resistances of \( p \)-MOS and \( n \)-MOS transistors.
Figure 11.2: The drain current versus input voltage of the NOT gate at different mode of operation

Owing to the input and output rise/fall times is not the same, both n-MOS and p-MOS transistors will be on for a short period of time as illustrated by the drain current versus input voltage plot of the NOT gate at point 3 shown in Fig. 11.2. At this instant, the input voltage is at mid-point voltage, which is also named as switching voltage. This voltage is between $V_{in}$ and $(V_{DD} - V_{tp})$. This results in additional short circuit current pulse from $V_{DD}$ to ground $V_{SS}$ and typically increases power dissipation of about 5 to 10.0%. The short circuit current pulse is illustrated in Fig. 11.3.

Figure 11.3: Graph showing the short circuit current when the input voltage is between $V_{in}$ and $(V_{DD} - V_{tp})$

As illustrated in Fig. 11.3, the short circuit current pulse occurred at two instants for a input pulse connected to the NOT gate. One occurs at logic 0 to logic 1
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transition and one occurs at logic 1 to logic 0 transition. The average short circuit current ($I_{SC}$) can be calculated using equation (11.5).

$$I_{SC} = \frac{\beta_{p} A_{off}}{12V_{DD}} (V_{DD} - |V_{TP}|)^3$$  \hspace{1cm} (11.5)

The average short circuit power dissipation ($P_{SC}$) is equal to

$$P_{SC} = \frac{\beta_{p} A_{off}}{12} (V_{DD} - |V_{TP}|)^3$$  \hspace{1cm} (11.6)

The second source of dynamic power dissipation ($P_{dyn}$) is the average dynamic power dissipation caused by charging and discharging of the load capacitance ($C_{out}$) shown in Fig. 4.4. The output is charged to $V_{DD}$ during transition to logic 1 and discharged to logic 0 during transition to logic 0. The sum of charging and discharging time is considered as equal to the period $T$ of the input frequency. Thus, the dynamic current $i_{DD}$ is equal to $Q/T$, where $Q$ is the charge of output capacitor $C_{out}$, which is also equal to $V_{DD}C_{out}$. The dynamic power $P_{dyn}$ is equal to

$$P_{dyn} = V_{DD}i_{DD} = V_{DD} \frac{Q}{T} = C_{out} V_{DD}^2 f$$  \hspace{1cm} (11.7)

Figure 11.4: Charging and discharging circuits of a NOT gate

The third main source of dynamic power dissipation is the glitching power. Glitching is defined as spurious and unwanted transitions that occur before a node settles down to its final steady-state value. It is caused by gate delay of the logic circuit during logic transition arises from paths with unbalanced
propagation delays converge at the same point in the circuit. It can be illustrated from the logic circuit function \( Q_2 = \overline{A + B - C} \) shown in Fig. 11.5. During the input transition from logic ‘010’ to ‘000’, due to the logic gate delay at output \( Q_1 \), it causes the glitch at output \( Q_2 \). The glitch will dissipate additional dynamic power of the logic circuit.

**Figure 11.5:** The figure showing glitching power dissipation due to gate delay

After adding the static power \( P_{DC} \), the total power dissipation \( P_D \) of the NOT gate is equal to

\[
P_D = V_{DD}I_{DDQ} + C_{out}V_{DD}^2f
\]  
(11.8)

In summary the power dissipation of the logic circuit comes from many sources. Source such as band-to-band tunneling, hot carrier injection, channel punch-through etc are not discussed here. As the results, the total power dissipation of the logic gate is given by

\[
P_D = V_{DD}I_{DDQ} + C_{out}V_{DD}^2f + P_{SC}
\]  
(11.9)

If we are to sum-up the various contribution of power dissipation of the logic gate, the static power contributes 10 to 25%, the charging and discharging dissipative power contributes 80%, and short-current power contribution approximately 10%. Based on these figures, there is an urgency to reduce the charging and discharging dynamic power dissipation for low power design.
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11.1.4 Power-Delay Product and Energy-Delay Product

Propagation delay $t_p$ and the power dissipation of the logic circuit are inter-related. Propagation delay is an important parameter because it decides the speed that a given amount of energy can be stored on the gate capacitor. The faster the energy transfers, the faster the gate. For a given technology and gate topology, the product of power dissipation and propagation delay is generally a constant. This product is called the power-delay product PDP. This parameter is considered as a quality measurement of the logic circuit. It is also defined as the energy consumed by the gate per switching event. Mathematically, the power-delay product PDP is equal to

$$\text{PDP} = P_{\text{dyn}} t_p$$

(11.10)

If the gate is switching at its maximum frequency, whereby $f_{\text{max}} = 1/(2t_p)$, then power-delay product is equal to

$$\text{PDP} = C_{\text{out}} V_{\text{DD}}^2 f_{\text{max}} t_p = \frac{C_{\text{out}} V_{\text{DD}}^2}{2}$$

(11.11)

An ideal gate should dissipate little energy. This can be done by many ways which will be discussed in next Section. However, implementing the energy reduction schemes, it may be with the expense of the performance of the logic circuit. Thus, a more relevant metric should be used to measure the performance of the logic circuit, which is combining a measurement of performance and energy named the energy-delay product EDP. The energy-delay product is defined as

$$\text{EDP} = \text{PDP} \cdot t_p = \frac{C_{\text{out}} V_{\text{DD}}^2}{2} t_p$$

(11.12)

11.2 Power Dissipation of Complex Logic Gate

The total power dissipation $P_D$ of the logic gate is $P_D = V_{\text{DD}} I_{\text{DDQ}} + C_{\text{out}} V_{\text{DD}}^2 f$ after ignoring the short circuit power dissipation. Since the static power $V_{\text{DD}} I_{\text{DDQ}}$ is small as compared to the dynamic power. Therefore, power dissipation of logic gate is basically come from dynamic power. Dynamic power is power consumption resulted from transistor switching from logic 0 to logic 1 and from logic 1 to logic 0. For a complex logic circuit that has many transitions and if we assume that there are equal chance of transition from logic 0 to logic 1 and vice versa, then we can introduce the term activity coefficient $a$, which is the
product of probability \( p_0 \) of transition from logic 0 to logic 1 and \( p_1 \) the probability of transition from logic 1 to logic 0. Thus, activity coefficient is \( a = p_0 p_1 \). The power dissipation of a gate can be written as

\[
P_D = aC_{\text{out}} V_{DD}^2 f
\]

Take for an example, a 2-input NOR has three logic 0 output and one logic 1 output, the activity coefficient is \( a = \frac{3}{4} \cdot \frac{1}{4} = \frac{3}{16} \). However, most of the digital system shows that the maximum activity coefficient is 0.5. Thus, in general equation (11.7) can be re-written as

\[
P_{\text{dyn}} = 0.5C_{\text{out}} V_{DD}^2 f
\]

For a complex circuit that contains \( N \) complex gate, the total power dissipation after ignoring static power dissipation is equal to

\[
P_D = \sum_{i=1}^{N} a_i C_i V_i V_{DD} f
\]

or

\[
P_D = \sum_{i=1}^{N} 0.5C_i V_i V_{DD} f
\]

### 11.2 Concepts of Low Power Circuit Designs

In this section, the concepts of how to design low power logic and digital circuits are studies. Two approaches will be presented namely the reduction based on the physical parameters of the device and the second approach is from the aspect of physical layout and operation of the integrated circuit.

#### 11.2.1 Physical Parameters of Device

From the studies of Section 11.1, four factors influencing low power design, which is depending physical parameters of the device, operation of the circuits, and the applied power supply, are identified. As you can from equation (11.14), which is \( P_D = aC_{\text{out}} V_{DD}^2 f \), the power dissipation of the circuit is depending on four factors, which are power supply \( V_{DD} \), load capacitance \( C_{\text{out}} \), activity coefficient \( a \), and operating frequency \( f \). Certainly, we would not like to look
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much at reducing operating frequency of the circuit as the mean to reduce the power dissipation. It is because circuit operating at low frequency would defeat the purpose of having high performance circuit. However, we can look non-critical part of the circuit to operate at lower frequency. Thus, it saves power dissipation. We will look at how to reduce the other three factors as the mean for low power design. These factors are inter-related that they would complicate the power optimization process. We will also be discussing another factor, which is the interconnect in this Section.

11.2.2 Voltage
The simple equation relating power $P$ and supply voltage $V_{DD}$ is $P = \frac{V_{DD}^2}{R}$. If there is a two folds reduction of power supply $V_{DD}$, it will reduce 4 folds in power dissipation. Thus, one can see that one of most effective mean for minimizing power dissipation of the circuit is to reduce supply voltage.

Power supply reduction is mandatory when the designer reduces the physical dimension of the device for achieving higher density of integration. The approach is used to develop sub-micron size device structures. Effects which are negligible in large MOS transistor become distinct and extremely important when the transistor dimensions are reduced. Scaling theory provides a general guide to make MOS transistor smaller. It is not possible or desirable to follow every aspects of the theory. However, it remains a useful metric for measuring progress in device physics especially the simulation or prediction of the behavior of the device with smaller dimension.

Scaling theory deals with the question of how the device characteristics are changed as the dimensions of the device are reduced in an idealized well-defined manner. Scaling theory is ideal ignoring many small-device effects that govern the performance of MOS transistor. It is often desirable to adhere to the large device models for simplicity but modify the parameters to account for the more important changes in the transistor parameters. Scaling of the device to smaller dimension affects parameters such as threshold voltage and mobility. Smaller channel length decreases the threshold voltage. Narrower device increases threshold voltage. Small channel length increases horizontal electric field that causes the MOS transistor to operate with saturation velocity. This reduces the drain current of the device. High electric field means high energetic carrier that can enter the oxide to become trapped charge and affects the threshold voltage of the MOS transistor. The drain and source of the MOS transistor are usually much heavily doped than the bulk. Couple with high electric field, hot ion tunneling is unavoidable. This issue causes leakage.
order to resolve this problem, lightly doped drain approach is adopted for the design of small dimension MOS transistor.

Several schemes can be constructed from scaling rules shown in Fig. 11.6. S is the dimensional scaling factor and k is factor by which voltages are scaled. One of the earlier scaling methodologies is based on constant-field scaling, which keep electrical field constant. In this method S is made equal to k. This approach is theoretical viable that has to increase the speed, reduction of voltage swing and capacitance. It is being used to scale to 1.0µm. Scaling to 1.0µm is in fact closed to constant-voltage scaling, which is by making k = 1. In this approach voltage swing stays the same, but device current increases due to increase of oxide capacitance $C_{ox}$. Since drive current increases roughly as the square of supply voltage, constant-voltage produces more speed improvement than constant-field scaling.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Variables</th>
<th>Scaling Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimensions</td>
<td>W, L, d$_{ox}$, x$_j$</td>
<td>1/$S$</td>
</tr>
<tr>
<td>Potentials</td>
<td>$V_{ds}$, $V_{gs}$</td>
<td>1/$k$</td>
</tr>
<tr>
<td>Doping concentration</td>
<td>N$_A$, N$_D$</td>
<td>$S^2$/$k$</td>
</tr>
<tr>
<td>Electric field</td>
<td>E</td>
<td>$S$/$k^2$</td>
</tr>
<tr>
<td>Current</td>
<td>$I_{ds}$</td>
<td>$S$/$k^2$</td>
</tr>
<tr>
<td>Gate delay</td>
<td>$t_{delay}$</td>
<td>$k$/$S^2$</td>
</tr>
</tbody>
</table>

**Figure 11.6:** Generalized scaling theory for MOS transistor

Using constant-voltage approach and considering a MOS transistor with a channel width $W$ and a channel length $L$ such that the channel area is $A = LW$ and introducing the concept of a scaling factor $S > 1$, a new scaled device is created with reduced dimensions $W'$ and $L'$ where $W' = \frac{W}{S}$ and $L' = \frac{L}{S}$. The reduced scaled area $A'$ is equal to $A' = \frac{A}{S^2}$. Similarly, the oxide thickness is $d'_{ox} = \frac{d_{ox}}{S}$. Thus, the reduced oxide capacitance is $C'_{ox} = S \cdot \frac{e_{ox}}{d_{ox}} = SC_{ox}$. Similarly, the reduced process parameter $K' = SK$ and device parameter is $\beta' = S\beta$. Threshold voltage $V'_t$ and drain-to-source voltage $V'_{ds}$ are to be scaled. With all parameters being scaled down, the scaled down drain current is $I'_D = \frac{I_D}{S}$.

Upon looking at the approach of voltage scaling for the device, let’s look at the effect of device after power supply reduction. Reduction of power supply
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$V_{\text{DD}}$ will drastically increase the timing of the circuit such as rise/fall time and propagation as the $V_{\text{DD}}$ voltage is approaching the threshold voltage $V_{t}$ of the device. The fall time follows equation

$$t_f = \frac{2.2C_{\text{out}}}{\beta_n (V_{\text{DD}} - V_{\text{i}})}$$

and rise time follows

$$t_r = \frac{2.2C_{\text{out}}}{\beta_p (V_{\text{DD}} - |V_{\text{ip}}|)}$$

These equations clearly indicate that the timing of the device is dependent on the difference of power supply voltage and threshold voltage of the device i.e. $(V_{\text{DD}} - V_{\text{i}})$ or $(V_{\text{DD}} - |V_{\text{ip}}|)$. This means that as the supply voltage $V_{\text{DD}}$ is reduced, the threshold voltage of the device has to be reduced in order to strike a balance between power supply reduction and timing optimization of the device. From the scaling theory, it is usually kept at the limit of $V_{\text{DD}}$ equal to 2 to 3 times of threshold voltage $V_{t}$.

Reducing the threshold voltage allows power supply voltage to be scaled down without loss in timing. The limit of how low the threshold voltage should be is set by the requirement to set adequate noise margin and the control in the increase in sub-threshold current leakage. The optimum threshold voltage must be determined based on the current drives at low power supply operation and control of the leakage current. Since the inverse threshold voltage slope of MOS transistor is invariant with scaling, for every reduction of 80 to 100mV in threshold voltage, the static current will be increased by one order of magnitude. This would limit the threshold voltage to 0.3V.

Power supply reduction also requires the support circuitry for low power operating such as buffer circuits and logic conversion circuits. This is because the ‘heart’ of the integrated circuit can be operating at power supply of 1.2V but power supply at the external world is not operating at 1.2V. It can be 3.3V in the case of microprocessor. Thus, it is necessary to have buffer circuits for capacitance matching and logic conversion circuits for changing switching point of the internal circuit that operates at 1.2V and vice versa at the output side operates at 3.3V.

11.2.3 Physical Capacitance

Dynamic power dissipation depends linearly on the physical capacitance being charged or discharged as it is shown in equation (11.7). So in additional to operating the circuit at low power, minimizing capacitance offers another technique for minimizing power dissipation of the circuit. The junction
capacitance is dependent of bias voltage, i.e. \( C_j = \frac{C_{om}}{1 + \frac{V_{DD}}{V_{bi}}} \), the drain/source capacitances are dependent on LTI factor i.e. 
\[
K_m(0, V_{DD}) = \frac{V_{bi}}{(-m+1)(V_{DD})} \left[ \left(1 + \frac{V_{DD}}{V_{bi}}\right)^{(-m+1)} \right],
\]
which is logic swing dependent, and the sidewall and bottom capacitances are width and length of the drain/source dependent. Thus, according scaling theory, reducing supply voltage (\( V_{DD} \)) with a must to reduce the dimension of the MOS transistor and logic levels would get smaller capacitance, which would improve timing and reduce power dissipation of the logic circuit.

Interconnect plays an increasing role in determining the total chip area and the number of level of design, timing, and power dissipation. Hence, it must be accounted for as early as possible during the design process. The inter-layer capacitance, which is governed by equation 
\[
C_{metal} = \frac{\varepsilon_{ox} LW}{X_{int}}
\]
can be small or large depending on the dimension and the type of dielectric material used (usually low k material is used not silicon dioxide for sub-micron design). In today’s sub-micron integrated circuit design, the thickness of the interconnect metal is usually thicker than the width of the interconnect. Thus, the sidewall electric fringes cannot be ignored for the calculation of interconnect capacitance. Based on the discussion, the interconnect capacitance estimation is however a difficult task even after technology mapping due to lack of detailed place and route information. Approximate estimates can be obtained by using information derived from a companion placement solution or by using stochastic/procedural interconnect models. Interconnect capacitance estimation after layout is straightforward and in general accurate.

In general and reality, estimating capacitance at the behavioral or logical levels of abstraction is difficult and immerse as it required estimation of the load capacitance structures which are not easily mapped out not shown in gate library because it is very much dependent on the physical layout of the chip.

### 11.2.4 Switching Activity

In addition to voltage and physical capacitance, switching activity also influences dynamic power dissipation. An integrated circuit chip may contain an enormous amount of physical capacitance like the case of memory chip. If there is no switching in the circuit then there is no dynamic power dissipated. The
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data activity determines how often switching occurs. There are two components of switching activity namely $f_{clk}$ determines the average periodicity of data arrivals and $E_{(sw)}$ determines how many transitions each arrival will generate. For circuits that do not experience glitching, $E_{(sw)}$ can be interpreted as the probability of the power consumed transition will occur during a single data period. However, the calculation of $E_{(sw)}$ is difficult as it depends not only on the switching activities of the circuit inputs and the logic function calculated by the circuit. It also depends on the spatial and temporal correlations among the circuit inputs. For certain logic styles, however, glitching can be an important source of signal activity. Glitching can cause a node to make several power dissipation transitions. It should be avoided whenever possible. The data activity $E_{(sw)}$ can be combined with the physical capacitance $C_{out}$ to obtain switched capacitance ($C_{sw}$) using equation (11.17).

$$C_{sw} = C_{out}E_{(sw)}$$

(11.17)

The switching capacitance also describes the average capacitance charged during each data period, which is equal to $1/f_{clk}$.

Calculation of the switching activity in a logic circuit is difficult as it depends on a number of circuit parameters and technology-dependent factors which are not readily available or precisely characterized. Some of these factors are input pattern dependence, delay model, logic function, logic style circuit structure, and statistical variation of circuit parameters. We shall leave to the student for further study.

11.2.5 Physical Layout and Operation of the Circuits

The physical layout and the way of operation can have significant effects in power dissipation of the circuit. A way to reduce the power dissipation is having good layout and floor plan that can significantly reducing switching capacitance. Good layout such as sharing diffusion nodes as much as possible will reduce capacitance. The un-contacted diffusions between series transistor are usually smaller than those much be contacted. This is a way to avoid. Inter-layer metal capacitance can be reduced if low k insulator between layers is used. Moreover, inter-layer capacitance is much reduced if the layout adopting the approach of alternative parallel and horizontal layout between layers. Reducing the length of polysilicon line is also a way to reduce the capacitance.

The power savings can be achieved by various static and dynamic power management techniques are very application dependent, but the saving can be
significant. The concept of separation of power line for high-speed high power and low-speed low power consumption groups is a technique. In the core of the device which contains 99.0% of the transistors, it is wise to use low power supply. For the interface circuit with external world, which can be with other device, high power supply is necessary. This is the concept of multiple voltage supply scheme.

In many synchronous applications, a lot of power is dissipated by the clock. The clock is the only signal that switches all the time and it usually has to drive a very large clock tree. Moreover in many cases the switching of the clock causes a lot of additional unnecessary gate activity. For that reason, circuits are being developed with controllable clocks. This means that from the master clock, based on operating conditions, other clocks are derived that can be slowed down or stopped completely with respect to the master clock. The clock circuit itself is partitioned in different blocks and each block is clocked with its own clock. The power savings that can be achieved this way are very application dependent but it can be significant. Power saving techniques that recycle the signal energies using the adiabatic switching principles rather than dissipating them as heat are already in certain applications where speed can be traded for lower power. Similarly, technique based on combining self-timed circuits with a mechanism for selective adjustment of the supply voltage that minimizes the power dissipation while still satisfying the performance constraints, is another good method.

Applying parallel and/or pipelining design to lower requirement frequency of operation is another approach for reducing power dissipation. Replacing a single functional unit with N parallel units allows each unit to operate 1/N the frequency. A multiplexer can be used to select in between the results. The voltage can be scaled down accordingly offering quadratic saving in power dissipation at expense of doubling the chip area. Replacing a single functional unit with an N-stage pipelined unit also reduces the amount of logic clock cycle at the expenses of more registers. Again the voltage-scale down can be used to offset the increase of power dissipation due to increase of register. The combination of parallel and pipelined design can get even better power reduction.

There are many other methods that can used to reduce the power dissipation of the logic circuit. Method such as design with variable threshold for CMOS MOS transistors is a good approach. In the case dynamic circuit design, low threshold voltage MOS transistors are used for reducing power dissipation in the operation mode of logic network, while the high threshold
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Voltage MOS transistor is used to design the standby-mode transistors that have low static power dissipation mainly due to low leakage current. On top of variable threshold design, the substrate of the transistor can be biased with different voltage during active mode and standby-mode. In this approach, during active mode the transistor is substrate bias with high voltage, while when it is at standby-mode, it is be biased with lower substrate voltage.

11.3 Low Power Logic Circuits

Based on the methods learnt to reduce the power dissipation of the logic/digital circuit, in this Section, we would like the student to learn the actual logic circuit designs. The logic design techniques are dynamic logic circuit, pseudo n-MOS gate logic design, pass-transistor design, and adiabatic logic. We will emphasize on the adiabatic logic design in details.

11.3.1 Low Power Dynamic Logic Circuits

Dynamic CMOS logic circuit provides a different approach to design high speed cascade circuit. This method eliminates slow p-MOS transistor and using clocking signal for both the operation of the circuit and data synchronization. The method would reduce the number of p-MOS transistor tremendously. Thus, it reduces the load capacitance $C_{out}$ leading to reduction of power dissipation. The general dynamic logic circuit is shown in Fig. 11.7.

![Figure 11.7: General circuit of dynamic circuit design](image)

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The timing signal $\phi$ is at logic 0, the capacitor $C$ is pre-charged to voltage $V_{DD}$. When timing signal $\phi$ is at logic 1, the dynamic circuit is in evaluation mode. Depending on the condition of the $n$-MOS transistor network, the charge in the capacitor may be maintained to provide logic 1 at output or discharged through the $n$-MOS transistor network to provide logic 0 at output. If it is necessary, the frequency of signal $\phi$ lower for further reduction of power dissipation.

The dynamic logic circuit design for function $f(A, B, C) = A \cdot B + \overline{C}$ is shown in Fig. 11.8. When timing signal $\phi$ is at logic 0, the capacitor $C$ is pre-charged to supply voltage $V_{DD}$. When timing signal $\phi$ is at logic 1, the dynamic circuit is in evaluation mode. Depending on the condition of the input $A$, $B$ and $C$, the charge in the capacitance is either maintained to provide logic 1 at output or discharged through the $n$-MOS transistor network to provide logic 0 at the output. One would see that if the input $C$ is at logic 1, the $n$-MOS transistor is switched on. Thus, it provides a discharging path for capacitance $C$. As the result, the output would provide logic 0. Likewise, the input either $A$ or $B$ is at logic 0. There is no discharging path for the capacitor $C$. Thus, the charge in the capacitor is maintained and provides logic 1 at the output. Based on the above analysis, the logic function $f(A, B, C) = A \cdot B + \overline{C}$ can be designed with dynamic circuit.

![Figure 11.8: Dynamic circuit for $f(A, B, C) = A \cdot B + \overline{C}$](image)

This circuit already has the reduction power concept utilized by reducing the number of $p$-MOS transistor to one. Moreover, depending on the fabrication...
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technology used, it may already have reduced supply voltage \( V_{DD} \) that has lower load capacitance \( C_{out} \) due to smaller dimensions. The active transistors of this circuit are \( n \)-MOS transistors. They are in standby-mode when the \( p \)-MOS transistors are not switched on. Thus, this circuit is dissipating minimum power in non-active mode. If we employ the method we learnt in previous Section, we can always designed the \( p \)-MOS transistor with higher threshold voltage than the \( n \)-MOS active transistors. This is because higher threshold voltage means lower leakage current knowing that the \( p \)-MOS transistors are switched momentarily only. The \( n \)-MOS transistors are the ‘core’ that would determine the outcome of the logic. Thus, it is necessary to reduce the static power dissipation by reducing the diffusion capacitance.

The threshold voltage of the MOS transistor is equal to

\[
V_{tn} = V_{tno} + \frac{\sqrt{2\epsilon_s qN_A}}{C_{ox}} \left( \sqrt{(2\phi_F + V_{SUB})} - \sqrt{2\phi_F} \right)
\]

for \( n \)-MOS transistor and for \( p \)-MOS,

\[
V_{tp} = V_{tpo} - \frac{\sqrt{2\epsilon_s qN_D}}{C_{ox}} \left( \sqrt{(2\phi_F + V_{SUB})} - \sqrt{2\phi_F} \right).
\]

This shall mean that if different substrate voltage is being used for active mode and standby-mode, it can help in power reduction. Normally the substrate of \( n \)-MOS transistor is biased with 0V. During the active mode, if the substrate voltage is biased with a negative voltage say -1.0V, the threshold voltage would reduce. This helps in power reduction. Normally, the \( p \)-MOS transistor is biased with supply voltage \( V_{DD} \). During the active mode, if the substrate voltage is biased a higher positive voltage say \( (V_{DD}+1.0)V \), the threshold voltage would reduce. This helps in power reduction.

11.3.2 Low Power Pseudo \( n \)-MOS Gate Logic Design

A complex logic circuit required equal number of \( n \)-MOS transistor and \( p \)-MOS transistor. This posts problem because of large area depicts less density design and consuming large amount power. To resolve these problems, the method is to keep the fast response \( n \)-MOS transistor network and replaces the \( p \)-MOS transistor network with a \( p \)-MOS pull-up network simply means connecting a \( p \)-MOS transistor with gate grounded as active load device. In this manner, the number of transistors especially the \( p \)-MOS transistor is reduced to one. The circuit is now named as pseudo \( n \)-MOS gate since it is derived from \( n \)-MOS technology. However, this circuit requires the condition \( \beta_n > \beta_p \). Otherwise, low output voltage \( V_{OL} \) value is difficult to be achieved due to threshold loss. This shall mean that the dimension of \( p \)-MOS transistor is designed to be smaller than the \( n \)-MOS transistor, which is good in terms power reduction. The most
significant disadvantage of using a pseudo $n$-MOS gate is the nonzero static power dissipation since the $p$-MOS transistor is always switched on and consumed power when the output is at logic 0. However, it may not be a real concern since it is only one $p$-MOS transistor is consuming power not a number of them like the case CMOS design.

Let’s consider a pseudo $n$-MOS inverter circuit shown in Fig. 11.9(a) and its corresponding voltage transfer characteristic VTC shown in Fig. 11.9(b).

![Figure 11.9: (a) A pseudo $n$-MOS inverter and (b) The voltage transfer characteristic of the inverter](image)

Since the output low voltage $V_{OL}$ is a concern, we shall look at the equation governing the calculation of $V_{OL}$. Without going into lengthy derivation, the $V_{OL}$ of the pseudo $n$-MOS logic circuit is equal to

$$V_{OL} = (V_{DD} - V_{in}) - \sqrt{(V_{DD} - V_{in})^2 - \frac{\beta_p}{\beta_n}(V_{DD} - |V_{tp}|)^2}$$

(11.18)

In order for the $V_{OL}$ value to be close to zero, which is the ideal case, the term $\frac{\beta_p}{\beta_n}(V_{DD} - |V_{tp}|)^2$ has to be as small as possible or $(V_{DD} - V_{in}) \gg \frac{\beta_p}{\beta_n}(V_{DD} - |V_{tp}|)^2$. Thus, this equation gives rise to the conditions $\beta_n > \beta_p$ and small $(V_{DD} - |V_{tp}|)$ are required, for low $V_{OL}$. This means voltage scaling technique can be used for saving power.

The sheet resistance of $p$-MOS transistor is about 2.5 times higher than the $n$-MOS transistor. As the rule of thumb, the resistance value of $p$-MOS transistor should be 5 times the resistance value of $n$-MOS transistor. This shall mean $(L/W)_p = 2(L/W)_n$. Applying the scaling theory appropriately, pseudo $n$-MOS logic circuit design is low power logic design.
The layout of a complex logic circuit function $(A \cdot B) + C$ design with pseudo $n$-MOS gate is shown in Fig. 11.10. Notice that the dimension of the $n$-MOS transistor network is larger than the grounded $p$-MOS transistor.

![Figure 11.10: Layout of a complex logic function $(A \cdot B) + C$ designed with pseudo $n$-MOS gate design concept](image)

The low power pseudo $n$-MOS logic design can be extended to design programmable logic array PLA that not only has low power dissipation but also has low switching activity. This device is originally created for standalone device that allows user to program for different functionality. However, the capability of PLA is limited and has been replaced by significantly more powerful field programmable gate arrays FPGA. Designer usually likes to develop PLA into a highly regular, multiple output structure for the ease of automatic layout generation. Indeed ready only memory ROM is also designed using this concept.

The block of a PLA is shown in Fig. 11.11. It consists of an input buffer that provides both non-inverting and inverting input and a two-level combinational circuits that provide sum-of-product logic functions. The “AND” block is responsible for generate product term and the “OR” is responsible for selection of product term to form the desire logic output.
The design examples of logic circuit using PLA is shown in Fig. 11.12.

The circuit consists of a 2-input AND gate, a 2-input NOR gate, and an exclusive OR gate. The input buffer provides the inverting and non-inverting logic, which are \( A, B, \overline{A}, \) and \( \overline{B} \). The row provides the product term. Row 1 shows the pseudo n-MOS \( A + \overline{B} \) gate, which is also the product term \( \overline{A} \cdot B \). Row
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2 shows the pseudo n-MOS \( \overline{A+B} \) gate, which is also the product term \( \overline{A} \cdot \overline{B} \). Row 3 shows the pseudo n-MOS \( \overline{A}+B \) gate, which is also the product term \( A \cdot \overline{B} \). Row 4 shows the pseudo n-MOS \( \overline{A}+B \) gate. Column 1 has a pseudo n-MOS inverter, whereby its input is connected to \( \overline{A+B} \), which will yield \( (A+B) \). However, after connected to an inverter, it yield back \( A+B \) logic. Column 2 has the input of the pseudo n-MOS inverter connected to \( (A \cdot B) \), which will result \( \overline{A} \cdot B \). However, after the inverter, it yields \( A \cdot B \) logic. Column 3 has a 2-input pseudo n-MOS NOR gate, whereby its inputs are respectively connected to \( \overline{A} \cdot B \) and \( A \cdot \overline{B} \), which would result exclusive NOR gate. However, after the inverter, it yields back exclusive OR logic.

11.3.3 Low Power Pass-Transistor Design

The logic design using pass-transistor has the advantage of reducing the number of transistor needed for the convention CMOS design. Thus, this design concept is a way to reduce the power dissipation of the logic circuit. A 2-input exclusive NOR with function is \( f(A, B) = \overline{A} \oplus B \) that can written as \( \overline{A} \cdot \overline{B} + A \cdot B \). The function can be designed by Oring two \( n \)-channel pass-transistors with an ANDing functions \( \overline{A} \cdot \overline{B} \) and \( A \cdot B \) respectively. The design of function is shown in Fig. 11.13.

Figure 11.13: Exclusive NOR gate design using \( n \)-channel pass-transistor
For this design, six transistors are needed instead of CMOS design that requires ten transistors. Scaling the supply voltage ($V_{DD}$) and dimension reduction can further reduce the power dissipation without the expense of speed since fast $n$-MOS transistors are used as pass-transistor.

The design of a 3-input AND gate with function $f(A, B, C) = A \cdot B \cdot C$ is shown in Fig. 11.14. This design is used to overcome threshold loss. The $p$-channel MOS transistors are used to pass logic 0, when either input B or C or both are at logic 0. Otherwise, the output will be at high impedance state or undefined state. In this design the number of transistor required is four instead of eight which is required for CMOS design.

![3-input AND gate design using $p$-channel and $n$-channel pass-transistors](image)

**Figure 11.14:** 3-input AND gate design using $p$-channel and $n$-channel pass-transistors

### 11.4 Adiabatic Logic Designs

Adiabatic logic is the term given to low-power electronic circuits that implement reversible logic. The term comes from the fact that an adiabatic process has the total heat or energy in the system remains constant. Designer knows the fact that as circuit getting smaller and faster, its energy dissipation greatly increases, which is a problem that adiabatic circuit can address.

With current CMOS technology, it is already fairly energy efficient and dissipates power as heat around 90% during switching. In order to reduce power dissipation during switching, it is by mean of adiabatic logic design. There are three fundamental rules that a CMOS adiabatic circuit needs to follow. The first
rule is never to switch on the transistor when there is a voltage difference between the drain and source of the transistor. This action may erase logic information and causes capacitive energy dissipation, which is equal to $\frac{1}{2} C_{\text{out}} V_{\text{DD}}^2$. The second rule is never to switch-off a transistor that has current flowing through it. This is because the switched-on transistor has relatively low channel resistance $R$ and low drain-to-source voltage ($V_{\text{DS}}$) across it. If it is being switched-off the channel resistance increase will cause voltage difference between drain and source, which is a violation of rule 1. The third rule is never suddenly change the voltage applied across any switched-on transistor. This is to avoid non-reverse transition because the transition will be more reversible energy dissipation. i.e. $C_{\text{out}} V_{\text{DD}}^2 f t$ not $\frac{1}{2} C_{\text{out}} V_{\text{DD}}^2$.

As we already know from the studies in earlier Section, CMOS transistors dissipate most of the power during switching. The main part of this dissipation is due to the need to charge and discharge the load capacitance $C_{\text{out}}$ through its channel resistance $R_p/R_n$. Thus, from equation (11.13), which is $aC_{\text{out}} V_{\text{DD}}^2 f$, the energy $E$ dissipated when charging is equal to

$$E = aC_{\text{out}} V_{\text{DD}}^2 f t$$

where $t$ is the time constant, which is equal to $C_{\text{out}} R_n$ or $C_{\text{out}}/R_p$. It is the time taken to charge or discharge. Thus, for non-reversible logic circuit, the charging/discharging time is proportional to $C_{\text{out}} R_p$ and $C_{\text{out}} R_n$ respectively.

Reversible logic uses the fact that the period $T$ of a single clock cycle is much longer then time constant. Thus, the intention is to spread the charging of the logic circuit over the whole cycle and it reduces the energy dissipated because longer time means lesser power dissipation. In order to extend the charging time of the logic circuit, the designer must observe the three rules mentioned earlier. He must make sure not to switch-on a transistor when it has a potential difference between its source and drain. Once the transistor is switched-on, energy flows through it should be in a gradual and controlled manner. The second rule is that once the current is flowing in the adiabatic circuits, it not be switched abruptly. It should be gradually changed from switch-on to switch-off when the voltage of the logic circuit changes. Beside, the change of switching speed should be proportional to the speed of gate voltage change. The third rule is never suddenly change the voltage applied across any switched-on transistor. With these rules followed, the transistor is in the undefined state for a long period of time, whereby during this time, the
voltage drop across the transistor is greatly reduced to almost zero and the resistance is very high. Thus, the circuit practically consumes little power or no power.

Throughout the years, many designs of adiabatic logic circuits have been developed. Among them are the Split-level Charge Recovery Logic SCRL, Glitch Free Cascadable Adiabatic Logic GFCAL, Two Level Adiabatic Logic 2LAL, Pass-Transistor Adiabatic logic PAL, and Complimentary Pass-Transistor Energy Recovery Logic CPERL etc. Most of the design relies heavily on the transmission gates, pass-transistor, uses trapezoidal wave to clock the circuit, and at time they can be fully pipelined. We shall discuss three types of design here, which are SCRL, 2LAL, and GFCAL. The rest of design types, we shall leave it to the student for further study.

### 11.4.1 Split Level Charge Recovery Logic

The Split level Charge Recovery Logic SCRL adiabatic logic is developed by T. Knight and S. Younis. The transistor level SCRL NAND gate is shown in Fig. 11.15. This transistor level circuit is same as the conventional CMOS NAND gate, with an additional transmission gate and a $p$-MOS transistor connected parallel with $n$-MOS transistor $A$. However, the main difference is power supply rail and the ground rail. They are driven by the trapezoidal clocks $\phi$ and $\bar{\phi}$ instead of supply voltage $V_{DD}$ and ground rail $V_{SS}$.

![Figure 11.15: A SCRL Adiabatic NAND gate](image)

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With the three rules for adiabatic logic operation are followed strictly. In the non-operational mode, the power rails of the logic circuit are set at \( V_{DD}/2 \) and the transmission are set at off mode, which is \( P_1 \) set to \( V_{SS} \) and \( \overline{P}_1 \) set to \( V_{DD} \). In the operational mode, the logic input \( A \) and \( B \) are set accordingly. The transmission gate is then switched-on by gradually switching the value of \( P_1 \) to logic 1 and \( \overline{P}_1 \) to logic 0. This is then following by changing the trapezoidal signal \( \phi \) and \( \overline{\phi} \) which are initially at \( V_{DD}/2 \) to \( V_{DD} \) and \( V_{SS} \) respectively. At this point, the logic circuit computes the NAND of \( A \) and \( B \) like a non-adiabatic gate would get. Once the output is used by the next stage of the circuit, the transmission gate is switched-off gradually. The trapezoidal signal \( \phi \) and \( \overline{\phi} \) are gradually returned to \( V_{DD}/2 \). The input \( A \) and \( B \) of the logic gate can now be changed for next logic cycle. It is important not to change the input until the rails are back to \( V_{DD}/2 \) so that a transistor is not switched on when there is a potential difference thus violating the first rule.

There is an extra \( p \)-MOS transistor connected to input \( B \). Let’s analyze the purpose of this transistor. Once trapezoidal signal \( \phi \) and \( \overline{\phi} \) are split to \( V_{DD} \) and \( V_{SS} \) and when the input \( A \) has logic 1 and input \( B \) has logic 0, current flows from \( V_{DD} \) through the \( p \)-MOS transistor controlled by input \( B \) and down through the \( n \)-MOS transistor controlled by input \( A \) which means that the \( n \)-MOS transistor barely turned on because at this instant, the voltage across \( n \)-MOS transistor is barely equal to \( V_{in} \). By adding the extra \( p \)-MOS will bypass the current to \( p \)-MOS transistor to ensure this internal node is not dissipating high energy. Thus, valid output logic 1 would be observed.

Finally the only node that is not restored by the gate is the output. This is doing so that a fully pipelined circuit at the gate level can be cascaded. Also, in order to achieve the gradual swings needed to operate these gates, trapezoidal signals are used so that initially, the voltage is held constant for quarter of a cycle, then gradually gets turned up or down, held constant again, and for the final quarter, is gradually returned to the initial value.

Using the SCRL adiabatic NAND logic circuit, we shall present the timing diagrams for the operation of this NAND gate. The timing is shown in Fig. 11.16. From the timing, it shows that it needs 1\( \frac{3}{4} \) cycle of clock signal to complete computing the output for the SCRL adiabatic NAND gate to show output logic 1. Unlike the CMOS NAND gate, the result is almost instantaneous.
Another interesting adiabatic circuit family is the Two Level Adiabatic Logic 2LAL developed by Michael Frank. Like SCRL, this family can be fully pipelined at the gate level. Figure 11.17(a) shows the basic building block of 2LAL consisting of a pair of transmission gates that transmit signal A and $\overline{A}$, and signal B and $\overline{B}$ respectively and having gate control $P$ and $\overline{P}$ respectively. The symbol representing both transmission gates is shown in Fig. 11.17(b). Notice that 2LAL logic design only requires transmission gate, which are one $p$-MOS transistor connect parallel to one $n$-MOS transistor.
Figure 11.17: The 2LAL basic gate

(a) 2LAL basic gate  (b) The symbol of 2LAL basic gate

Figure 11.18 shows the basic buffer element design with 2LAL adiabatic logic, which consist of two sets of transmission gates. $\phi_1$ and $\phi_0$ are both trapezoidal clock signal but $\phi_1$ is a quarter cycle behind $\phi_0$. Initially all the nodes are at 0. As the input gradually raises to logic 1 or stays at logic 0, the clock signal $\phi_0$ begins to transition to logic 1. On the next step, clock signal $\phi_1$ transitions to 1, which sets the output to 1 if the input is logic 1 and otherwise it is at logic 0, in which itself reduces the power dissipation because no charge passes through the transistor. On the third step $\phi_0$ transitions back to 0 resetting the input to 0. Finally $\phi_1$ transition back to 0 and the output is restored to 0 by the following gate in order to accommodate for full pipelining and thus the circuit is ready to process a new input.

The timing diagram of the operation of 2LAL buffer circuit is shown in Fig. 11.19. It takes two clock cycles to complete the operation of this buffer circuit.
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Figure 11.18: The 2LAL buffer circuit

Figure 11.19: The timing diagram for the operation of 2LAL buffer circuit
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11.4.3 Glitch Free Cascadable Adiabatic Logic

Glitch Free Cascadable Adiabatic Logic GFCAL inverter circuit is consists of a \( p \)-MOS transistor \( T_1 \) and a diode \( D_1 \) in parallel with an \( n \)-MOS transistor \( T_2 \) and a diode \( D_2 \), which in turn are connected in series with a capacitor \( C \). The supply voltage \( V_{DD} \) is a slowly varying triangular voltage. The \( p \)-MOS transistor \( T_1 \) and diode \( D_1 \) provide a charging path, and the \( n \)-MOS transistor \( T_2 \) and diode \( D_2 \) provide a discharging path for the load current. Figure 11.20 shows an inverter designed with glitch free cascadable adiabatic logic.

![GFCAL inverter circuit diagram](image)

**Figure 11.20:** A GFCAL inverter gate

When the input is logic 0, transistor \( T_1 \) is switched-on and transistor \( T_2 \) is switched-off. Transistor \( T_1 \) and diode \( D_1 \) allow the current to flow from the supply voltage to charge the capacitor \( C \) closed to the peak value of \( V_{DD} \) producing logic 1. The diode \( D_1 \) does not allow discharge into the supply when supply voltage \( V_{DD} \) is less than the output voltage, which is also the voltage across the capacitor \( V_C \).

When the input is logic 1, transistor \( T_2 \) is switched-on mode and transistor \( T_1 \) is switched-off ode. Diode \( D_2 \) and transistor \( T_2 \) starts to conduct. The diode \( D_2 \) prevents charging of the capacitor since it is reverse biased when supply voltage \( V_{DD} \) is greater than the voltage of capacitor \( V_C \) and allows only discharging of the capacitor back into the supply when supply voltage \( V_{DD} \) is less than voltage of capacitor \( V_C \). Thus, the capacitor voltage is brought down to
a low value when the input is high irrespective of the previous output. Hence, the output is the complement of the input. The output voltage level is almost independent of the time at which the input voltage is applied with respect to the supply voltage as long as it is applied at a time before $V_{DD}$ reaches the peak value.

From the derivation of the expression of energy consumed during charging and discharging of capacitor C, it shows that the energy dissipated decreases as time $T$ increases, where $T$ is time taken to ramp the supply voltage from zero volt to $V_{DD}$. Hence, the energy dissipated decreases with slowly varying the supply voltage.

We shall now look at how to design other logic gate such as NAND gate and NOR so that we can cascading these gates into in other combinational or sequential logic circuit such as the adder, exclusive NOR gate, D-latch etc. A two-input GFCAL NAND gate circuit is shown in Fig. 11.21.

![Figure 11.21: A two-input GFCAL NAND gate](image)

The NAND gate circuit consists of two $p$-MOS transistor $T_5$ and $T_6$ in parallel and a diode $D_3$ in series. The second branch consists of two $n$-MOS transistor $T_7$ and $T_8$ in series with a diode $D_4$. The two parallel branches are connected in series with a capacitor C. The supply voltage for the gates is $V_{DD}$, which is a slowly varying triangular voltage.
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A two-input GFCAL NOR gate circuit is shown in Fig. 11.22. The circuit consists of two branches in parallel. The first branch consists of two p-MOS transistor T₁, T₂ and a diode D₁ in series. The second branch consists of two n-MOS transistor T₃, T₄ in parallel, connected in series with a diode D₂. The two parallel branches are connected in series with a capacitor C.

![A two-input GFCAL NOR gate](image_url)

**Figure 11.22: A two-input GFCAL NOR gate**

11.4.4 Problems of Adiabatic Logic Designs

We have studied three methodologies of adiabatic logic designs. Now we would like to focus on the problem associated with this design. They are very slow circuits by today’s standards. It requires 50% more area than conventional CMOS circuit and simple circuit designs can be very complicated.

Perhaps, the ways to resolve the problem of speed can be by scaling to decreases R and C, which would naturally make evaluation time T to be smaller, hence increase the speed. Designer can employ multiple power-clock designs to handle pipelining that would enhance speed. New Technology such as Single-Phase Source-Coupled Adiabatic Logic SCAL that eliminates dc lines can enhance speed.
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11.1. Calculate the sub-threshold current of an n-MOS transistor that has the following parameters. \( V_t = 0.4 \text{V} \), \( \beta_n = 5.0 \times 10^{-4} \text{A/V}^2 \), \( V_{GS} = 1.0 \text{V} \), \( V_{DS} = 1.0 \text{V} \), \( V_T = 26.0 \text{mV} \), \( \eta = 5.0 \), and \( V_{DD} = 2.4 \text{V} \).

11.2. Using the data shown in Question 11.1, calculate the instantaneous dynamic power dissipation of the n-MOS transistor when its input voltage is at mid-point voltage.

11.3. A VLSI digital system has 20 million transistors using static CMOS for the logic gates with average activity coefficient of 0.2. The gate dimension of the transistor is 12\( \lambda \)\times 2\( \lambda \) and these transistors are fabricated using 0.12\( \mu \text{m} \) technology and operated at 1.2V \( V_{DD} \). If the capacitance of the gate is 0.2fF per \( \mu \text{m}^2 \), what is the dynamic power dissipation of the digital system, when its operating frequency is 1.0GHz?

11.4. Describe how a dynamic logic circuit designed with variable threshold voltage can help to reduce the power dissipation of the circuit.

11.5. Name three methods employ in VLSI design that can help to reduce the power dissipation.

11.6. Design a logic circuit function \( \overline{\text{Output}} = (\overline{A+B}) \cdot C \) using SCRL adiabatic design methodology.

11.7. Design a logic circuit function \( \overline{\text{Output}} = (\overline{A+B}) \cdot C \) using GFCAL adiabatic design methodology.

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