5.0 Introduction

The metal oxide semiconductor field effect transistor MOSFET a voltage control current device. It differs from junction field effect transistor JFET that it has no \textit{pn} junction structure. It has a metal gate, which insulates the conducting channel with silicon oxide \( \text{SiO}_2 \). In the modern design, metal gate has been replaced by either \( p^+ \) or \( n^+ \) polysilicon.

There are two types of MOSFET namely depletion-enhancement DE and enhancement E types. Figure 5.1 and 5.2 show the difference between the types.

The DE type has a narrow channel adjacent to the gate connecting the drain and source of the transistor. It can operate in either depletion mode or enhancement mode. The mode of operation is like the JFET.

The E type does not have a narrow connecting channel. It operates by forming a conducting channel of the same type like the source and drain. The channel is formed either by attracting electron or depleting away electron to form an \( n \)-channel or \( p \)-channel connecting the source and the drain.

MOSFET not only can be used to design amplification circuit. It can also be used as a capacitor and a resistor. This capability makes the VLSI design simpler because there is no need to use other element for capacitor and resistor in the design.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{mosfet.png}
\caption{The structure of depletion-enhancement \textit{n}-channel and \textit{p}-channel MOSFET}
\end{figure}
The symbol of both depletion-enhancement and enhancement MOSFET types are shown in Fig. 5.3 and 5.4 respectively. Note that for most cases, by design the substrate is connected to the source.

Symbols other then those symbols shown in Fig. 5.3 and 5.4 are used too. The reader needs to identify them careful during any circuit analysis. Circuit examples shown in this chapter will use any symbol listed in Fig. 5.3 and Fig. 5.4 as illustration.
5.1 Depletion-Enhancement MOSFET and Enhancement MOSFET

The transfer characteristic of depletion-enhancement DE and enhancement E MOSFETs are shown in Fig. 5.5 and 5.6 respectively.

The characteristic curve of DE type is same as the JFET except there is an additional enhancement part, where the curve extends to positive $V_{GS}$ i.e. attract either hole or electron. In depletion mode, electron in $n$-channel or hole in $p$-channel is depleted away. In enhancement mode, electron is attracted in $n$-channel and hole in $p$-channel.

![Transfer characteristic of DE MOSFET](image)

(a) $n$-channel  
(b) $p$-channel

**Figure 5.5:** Transfer characteristic of DE MOSFET

The equation for the transfer characteristics of depletion-enhancement DE MOSFET is same the JFET which is

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2$$

(5.1)

where $I_{DSS}$ is normally given by data sheet. If the design parameters are given then $I_{DSS}$ is defined as

$$I_{DSS} = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} V_{GS(\text{off})}^2$$

(5.2)
where \( L \) is channel length, \( W \) is width of the gate, \( C_{ox} \) is capacitance of oxide per unit area, and \( \mu_n \) is the effective mobility of electron, which has a nominal value \( 650 \text{cm}^2/\text{V-s} \) at \( 25^\circ \text{C} \).

Enhancement MOSFET uses only channel enhancement. If the drain and source are \( n \)-type, the gate is biased with positive voltage to attract electron from the substrate near the oxide to form an \( n \)-type conducting channel. Likewise, \( p \) MOSFET type has \( p \)-type drain and source, the gate is biased with negative voltage to form a \( p \)-type conducting channel.

![Figure 5.6: Transfer characteristic of E MOSFET](image)

There is a minimum gate-to-source voltage to be applied before conducting channel can be formed. This gate-to-source voltage is called \textit{threshold voltage} and is denoted as \( V_{GS(th)} \).

The threshold voltage \( V_{GS(th)} \) is used to overcome the flat band potential, surface potential, fixed charge, and oxide capacitance \( C_{ox} \) of the gate before inversion can be occurred.

A typical \( I_D-V_{DS} \) characteristic curve of an \( n \)-channel MOSFET for the selected \( V_{GS} \) is shown in Fig. 5.7. There are three regions - the cut-off region, the triode region (or almost linear region) and saturation region (operation region). The saturation region is the useful region for an amplifier operation, whereas the other regions are good for switch operation. The curve also shows
that the output impedance is infinite, which is not true in reality. We shall
discuss how to determine the finite output resistance later in the chapter.

![Figure 5.7: $I_D - V_{DS}$ characteristic curve of an $n$-channel MOSFET](image)

There are two equations of the transfer characteristics for enhancement
MOSFET.

At linear region, the equation is

$$I_D = 2K \left( V_{GS} - V_{GS(th)} \right) V_{DS} - \frac{1}{2} V_{DS}^2$$  \hspace{1cm} (5.3)$$

This equation is useful for MOSFET operating as a switch or digital device. We
would not use it at the time being since we are interested with operation region.

At saturation region (operation region), the equation is
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\[ I_D = K \left[ V_{GS} - V_{GS(th)} \right]^2 \]  \hspace{1cm} (5.4)

where \( K = \frac{I_D}{\left[ V_{GS} - V_{GS(th)} \right]^2} \), which can be calculated based on the known value of \( I_D \) for given \( V_{GS} \) and \( V_{GS(th)} \).

If the design parameters of the E MOSFET such as its channel length \( L \), width of the gate \( W \), and the capacitance of oxide \( C_{ox} \) are known then

\[
K = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} = \frac{1}{2} \beta
\]

where \( \mu_n \) is the effective mobility of electron which has value 650 cm\(^2\)/V-s and \( \mu_p \) is the mobility of hole which has 200 cm\(^2\)/V-s. \( W/L \) is called the aspect ratio for a given MOSFET. \( \beta \) is the intrinsic transconductance parameter usually specified in SPICE MOSFET’s model.

Differentiating equation (5.4) for drain current \( I_D \) with respect to gate-to-source voltage \( V_{GS} \) for a fixed drain-to-source voltage \( V_{DS} \) yields the transconductance \( g_m \) of the MOSFET.

Therefore,

\[
g_m = \frac{dI_D}{dV_{GS}} = 2K \left[ V_{GS} - V_{GS(th)} \right]
\]

or

\[
g_m = \frac{dI_D}{dV_{GS}} = \frac{2I_D}{\left[ V_{GS} - V_{GS(th)} \right]} \hspace{1cm} (5.6)
\]

**Example 5.1**
The data sheet for a certain enhancement MOSFET states that drain current is \( I_D = 3 \) mA at \( V_{GS} = 10 \) V and \( V_{GS(th)} = 5 \) V. Determine the drain current \( I_D \) for \( V_{GS} = 8 \) V.

**Solution**
From equation (5.4), \( K = \frac{3 \text{mA}}{(10 \text{V} - 5 \text{V})^2} = 0.12 \text{mA/V}^2 \)
Thus, the drain current $I_D$ at $V_{GS} = 8\, \text{V}$ is $I_D = 0.12\, \text{mA} / \sqrt{\text{V}^2 [8\, \text{V} - 5\, \text{V}]} = 1.08\, \text{mA}$.

**Example 5.2**
The $n$-channel MOSFET shown in the figure operates with drain current $I_D = 0.4\, \text{mA}$ and $V_D = 1.0\, \text{V}$. The transistor has $V_{GS(th)} = 2.0\, \text{V}$, $\mu_nC_{ox} = 20\, \mu\text{A/}\sqrt{\text{V}^2}$, $L = 10\, \mu\text{m}$ and $W = 400\, \mu\text{m}$. Determine its drain resistance $R_D$ and source resistance $R_S$.

**Solution**
Equation (5.4) is used to determine the $V_{GS}$ for $I_D$ current equal to 0.4mA. Thus, an equation $0.4 \times 10^{-3} = \frac{1}{2} \frac{20 \times 10^{-6}}{400} \frac{400}{10} (V_{GS} - 2)^2$ is obtained. Solving this equation yields two values for gate-to-source voltage, which are $V_{GS} = 1.0\, \text{V}$ or $3.0\, \text{V}$. Since $V_{GS(th)} = 2.0\, \text{V}$, gate-to-source voltage $V_{GS}$ should be $3.0\, \text{V}$.

$V_{GS} = V_G - V_S = 3.0\, \text{V}$ and $V_G = 0$, therefore $V_S = -3.0\, \text{V}$.

The source resistance is $R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-3 - (-5)}{0.4 \times 10^{-3}} = 5\, \text{k}\Omega$

and

the drain resistance is $R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5 - 1}{0.4 \times 10^{-3}} = 10\, \text{k}\Omega$
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5.2 Biasing of MOSFET

Figure 5.8 shows the biasing configuration of an \( n \)-channel and a \( p \)-channel MOSFET. For \( n \)-channel type MOSTFET NMOS, the gate is biased with positive voltage and the drain is biasing with positive voltage. For \( p \)-channel MOSFET PMOS, the gate is biased with negative voltage and the drain is biased with negative voltage. Note that the source is always common to both the gate-to-source and collector-to-source terminals.

\[ \text{Drain} \]
\[ \text{Gate} \]
\[ V_{GS} \]
\[ V_{DS} \]
\[ \text{Source} \]

(a) \( n \)-channel biasing configuration

\[ \text{Drain} \]
\[ \text{Gate} \]
\[ V_{GS} \]
\[ V_{DS} \]
\[ \text{Source} \]

(b) \( p \)-channel biasing configuration

Figure 5.8: Biasing configuration of an \( n \)-channel and a \( p \)-channel MOSFET

**Notation**

The current flow between drain and source is termed drain or source current \( I_D \) or \( I_S \). The voltage at source is denoted as \( V_S \), at drain is denoted as \( V_D \), and at gate is denoted as \( V_G \). The output resistance of MOSFET is denoted as \( r_o \) and the drain-source resistance is denoted as \( r_{DS} \).

5.2.1 Depletion-Enhancement MOSFET Biasing

A simple normal biasing method for depletion-enhancement MOSFET is by setting gate-to-source voltage equal to zero volt i.e. \( V_{GS} = 0V \). This method of biasing enables ac signal to vary the gate-to-source voltage above and below this bias point as shown in Fig. 5.9.
A depletion and enhancement MOSFET biased with $V_{GS} = 0$ is shown in Fig. 5.10.
Example 5.3
Using the circuit shown in Fig. 5.10, determine the drain current $I_D$ and drain-to-source voltage $V_{DS}$ given that $V_{GS(\text{off})} = -8V$, $I_{DSS} = 12mA$, $V_{DD} = 15V$, $R_G = 10M\Omega$ and $R_D = 600\Omega$.

Solution
From equation (5.1) the drain current is

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2$$

Since $V_{GS} = 0V$ then

$$I_D = I_{DSS} = 12.0mA$$

$$V_{DS} = V_{DD} - I_D R_D = 15.0V - 12mA(600\Omega) = 7.8V$$

5.2.2 Enhancement MOSFET Biasing

There are two standard methods that E MOSFET can be biased, which are shown in Fig. 5.11.

(a) Drain-feedback bias
(b) Voltage divider bias

For drain feedback bias, the gate has very high impedance and negligible gate current. Therefore, the voltage drops across $R_G$ is negligible. i.e. $V_{DG} \equiv 0$. Since $V_{DS} = V_{GS} + V_{DG}$, thus, $V_{GS}$ is equal to $V_{DS}$. 
For voltage-divider bias, \( V_{GS} = \frac{R_2}{R_1 + R_2} V_{DD} \). The voltage value is also equal to voltage at gate \( V_G \) since voltage at source \( V_S = 0 \).

**Example 5.4**

If a \( V_D \) voltage of 0.1V needs to be established for the design, what will be the value of \( R_D \) and effective resistance \( r_{DS} \) between drain and source of this NMOS? Given that \( V_{GS(th)} = 1V \) and \( K = 1.0mA/V^2 \).

\[
V_{DD} = 5\, V
\]

\[
V_D = 0.1\, V
\]

**Solution**

Since \( V_D = 0.1V \), this shall mean that \( V_{DS} = 0.1V \). This is also mean that the NMOS is operating at linear region because \( V_{DS} \leq (V_{GS} - V_{GS(th)}) \) - Refer to Fig. 5.7 Thus, from equation (5.3),

\[
I_D = 2K \left[ (V_{GS} - V_{GS(th)})V_{DS} - \frac{1}{2} V_{DS}^2 \right]
\]

\[
= 2 \times 10^{-3} \, A/V^2 \left[ (5 - 1) \times 0.1 - \frac{1}{2} \times 0.01 \right] = 0.79mA
\]

The required drain resistance \( R_D \) value is

\[
R_D = \frac{V_{DD} - V_{DS}}{I_D} = \frac{5V - 0.1V}{0.79mA} = 6.2k\Omega
\]
The effective resistance across the drain and source $r_{DS}$ is

$$r_{DS} = \frac{V_{DS}}{I_D} = \frac{0.1V}{0.79mA} = 174.5\Omega$$

**Example 5.5**

Given that drain current is $I_D = 0.4mA$, gate-to-source threshold voltage is $V_{GS(th)} = 2V$, $\mu_nC_{ox} = 20\mu A/V^2$, aspect ratio is 10, calculate the value for resistance $R$, drain voltage $V_D$, and effective channel resistance $r_{DS}$.

\[ V_{DD} = 10\ V \]

\[ I_D \]

\[ R \]

\[ V_D \]

**Solution**

The gate and drain are tied together, therefore drain-to-gate voltage is $V_{DG} = 0$ V. The NMOS is operation in saturation region since $V_{DS} > V_{GS} - V_{GS(th)}$. Thus, saturation equation (5.4) is used for calculation.

$$I_D = K[V_{GS} - V_{GS(th)}]^2$$

$$0.4mA = \frac{1}{2} \cdot 20 \times 10^{-6} A/V^2 \cdot 10[V_{GS} - 2]^2$$

From the equation, it yields two values for gate-to-source voltage i.e. $V_{GS} = 0$ or $4V$. Since the threshold voltage $V_{GS(th)}$ is $2.0V$, therefore the gate-to-source voltage $V_{GS}$ is $4.0V$.

$$V_{DS} = V_{D} - V_{S} = 4.0V$$
\[ R = \frac{V_{DD} - V_D}{I_D} = \frac{10V - 4V}{0.4mA} = 15k\Omega \]

\[ R_{DS} = \frac{V_D}{I_D} = \frac{4.0V}{0.4mA} = 10.0k\Omega. \]

**5.3 MOSFET as a Capacitor**

If the MOSFET is biased in accumulation mode, the MOS of MOSFET is acted as capacitor. The insulator oxide layer between the gate and the channel forms a parallel capacitor plate where its capacitance \( C_i = \frac{\varepsilon_i LW}{d_i} \), where \( LW \) is the cross sectional area, \( d_i \) oxide thickness and \( \varepsilon_i \) the permittivity of oxide.

**5.4 MOSFET as a Resistor**

If a MOSFET is connected as shown in Fig. 5.12, it has a variable resistance, which depends on the \( V_{GS} \) and \( V_{DS} \) bias. The ac resistance shall be \( \frac{1}{g_m} || \frac{r_o}{g_m} \).

![Figure 5.12: MOSFET connected as resistor and its characteristic](image)

**5.5 Small Signal Amplifier**

The transfer characteristic curve for depletion-enhancement MOSFET DE MOSFET is shown in Fig. 5.10. The Q-point is set at \( V_{GS} = 0 \) so that ac signal can be varied the gate-to-source above and below this Q-point.
The transfer characteristic curve for enhancement MOSFET is shown in Fig. 5.13. The Q-point of E MOSFET cannot be laid on drain current I_D axis because E MOSFET requires a minimum V_{GS} voltage, which is termed as threshold voltage V_{GS(th)} in order for operation.

Figure 5.13: Transfer characteristics curve for enhancement MOSFET

### 5.5.1 Equivalent Circuit for Enhancement MOSFET

From Fig. 4.14 of JFET equivalent circuit in Chapter 4, the output resistance r_o of MOSFET is at least a few orders higher than the drain resistance R_D. Similar it is true for MOSFET.

Practically there is no gate-to-source current. Thus, the gate-to-source resistance R_{in(gate)} is extremely high such that it can be treated as open circuit, which is similar like the JFET. Thus, the ac equivalent circuit of MOSFET is similar to the JFET.

Showing here is a number of equivalent circuits, which are useful for determining the small signal ac voltage gain later on. Fig. 5.14 and Fig. 5.15 show the equivalent circuits.
5.5.2 Finite Output Impedance of MOSFET

Reference to the graph shown in Fig. 5.7, it states the drain current $I_D$ is independent of drain-to-source voltage $V_{DS}$ at saturation (at the beginning of pinch-off) which shall mean that MOSFET has infinite output impedance $r_o$. In reality this is not true. Theoretically, at pinch-off, the channel shape and pinch-off point do not change upon further applying drain-to-source voltage $V_{DS}$. In reality the shape of channel changed and pinch-off point moved away from the drain. The change modifies the effective channel length of the device, which is termed *channel length modulation*. The illustration is shown in Fig. 5.16.
The voltage drop across the channel is \( V_{DS_{Sat}} = V_{GS} - V_{GS(th)} \). Any increase of \( V_{DS} \) voltage beyond \( V_{DS_{Sat}} \) (\( V_{DS} - V_{DS_{Sat}} \)) will drop across \( \Delta L \). This causes acceleration of electron from the channel to drain. From equation (5.4), \( I_D \) is inversely proportional to the channel length \( L \). Since channel length \( L \) decreases, \( I_D \) current increases. Equation (5.4) shall then be modified to

\[
I_D = \frac{\mu_n C_{OX} W}{2L} \left( V_{GS} - V_{GS(th)} \right)^2 \left( 1 + \lambda V_{DS} \right),
\]

where \( \lambda = 1/V_M \) and \( V_M \) is the Early voltage, which can be ranged from 20 to 200V. Figure 5.17 illustrates how Early voltage \( V_M \) can be determined.

**Figure 5.16:** Channel modulation caused by further increase of \( V_{DS} \) beyond pinch-off \( V_{DS_{Sat}} \) saturation voltage \( V_{DS_{Sat}} \)

**Figure 5.17:** The graph shows the Early voltage point
The graph in Fig. 5.17 shows that the output impedance \( r_o \) of the MOSFET is now having a finite value, which can be defined as
\[
r_o = \frac{\partial V_{DS}}{\partial I_D} \bigg|_{V_{GS} = \text{constant}} = \frac{V_{M} + V_{DS}}{I_D} \approx \frac{V_{M}}{I_D} \quad \text{for a fixed } V_{GS} \text{ voltage after neglecting small } V_{DS} \text{ voltage.}
\]

### 5.5.3 Analysis of MOSFET Amplifier

The amplifier configurations for MOSFET are same like the JFET's. The analysis of small-signal amplifier for DE and E MOSFET is same like JFET. Instead of repeating the procedure of analysis, examples are used as illustrations.

**Example 5.6**

A common-source amplifier shown in figure using a NMOS has \( I_D = 5 \text{mA} \) at \( V_{GS} = 7.5 \text{V}, \ V_{GS(th)} = 5 \text{V}, \ g_m = 6 \text{mS}, \ V_{in} = 48 \text{mV rms}, \) and \( V_M = 50 \text{V}. \) Find \( V_{GS}, \ I_D, \ V_{DS}, \ r_{DS}, \ R_{in}, \ V_{out} \) and ac voltage gain.

![Diagram of a common-source amplifier](image)

**Figure 5.18: A common source amplifier**

**Solution**

Since the source is grounded, the gate-to-source voltage is
\[
V_{GS} = \left( \frac{R_2}{R_1 + R_2} \right) V_{DD} = \left( \frac{33k\Omega}{33k\Omega + 47k\Omega} \right) 15V = 6.19V
\]
Using equation (5.4), substitute $V_{GS} = 7.5V$ and $V_{GS(th)} = 5.0V$, and $I_D = 5.0mA$ to determine the $K$ values of the MOSFET, which is $I_D = K\left[V_{GS} - V_{GS(th)}\right]^2$. Thus, the $K$ value is $K = 5mA/[7.5V - 5V]^2 = 0.8mAV^{-2}$.

The drain current $I_D$ at $V_{GS} = 6.19V$ is $I_D = 0.8mAV^{-2}[6.19V - 5V]^2 = 1.13mA$.

The drain voltage is $V_D = V_{DS} = 15V - 1.13mA \times 3.3k\Omega = 11.26V$. The drain-to-source resistance $r_{DS}$ is $r_{DS} = V_{DS}/I_D = 11.26V/1.13mA = 9.96 \, k\Omega$.

The ac equivalent circuit of the amplifier is shown in figure below.

![Figure 5.19: ac circuit of a common source amplifier](image)

The input impedance $R_{in}$ is equal to $R_1||R_2 = 47.0k\Omega||33.0k\Omega = 19.4k\Omega$.

The output impedance $r_o$ is $r_o = V_A/I_D = 50V/1.13mA = 44.6k\Omega$.

The output voltage is $V_{out} = -g_mV_{gs}(r_o||R_D) = 6.0mS \times 3.07k\Omega \times V_{gs} = 18.4V_{gs}$.

The input voltage is $V_{in} = V_{gs}$.

Therefore, the ac voltage gain is $A_V = V_{out}/V_{in} = -18.4V_{gs}/V_{gs} = -18.4V/V$.

The output voltage is $V_{out} = -A_VV_{in} = -18.4 \times 48mV \text{ rms} = -0.874V \text{ rms}$.

**Example 5.7**

Calculate the ac voltage gain $A_v$ and input impedance $R_{in}$ of the amplifier circuit shown in figure. Given that $K = 0.125mA/V^2$, threshold voltage $V_{GS(th)} = 1.5V$, and Early voltage $V_M = 75.0V$. 

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Solution

The ac equivalent circuit is shown in figure.

Using equation (5.4), which is

\[ I_D = K [V_{GS} - V_{GS(th)}]^2 \]

The drain current \( I_D \) is \( I_D = 0.125 \text{mA} / V^2 [V_{GS} - 1.5]^2 \)

Also, the drain voltage \( V_{DS} \) is \( V_{DS} = 15V - I_D \times 10.0k\Omega \).
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Since there is no current flow into the gate, the voltage across drain and gate shall be zero, thus, gate-to-source voltage is equal to drain voltage i.e. $V_{GS} = V_{DS}$.

Solving the above two equations, the drain current is $I_D = 1.06 \text{mA}$ and drain voltage is $V_{DS} = 4.4 \text{V}$.

Using equation (5.3), which is equation $I_D = K \left( V_{GS} - V_{GS(th)} \right)^2$. Differentiating this equation to obtain transconductance, which is $g_m \approx 2K \left( V_{GS} - V_{GS(th)} \right) = 2 \times 0.125 \text{mA} / V^2 \left( 4.4 \text{V} - 1.5 \text{V} \right) = 0.725 \text{mS}$

The output impedance of the MOSFET is $r_o = V_M / I_D = 75 \text{V} / 1.06 \text{mA} = 67.9 \text{k\Omega}$

The ac voltage gain $A_V$ is

$$A_V = -g_m (R_L \| r_o \| R_D) = -0.725 \text{mS} \times 4.66 \text{k\Omega} = -3.37 \text{V/V}$$

From the ac equivalent circuit shown in Fig. 5.21, the input current $i_i$ is

$$i_i = (V_{in} - V_{out}) / R_G$$

The input impedance $R_{in}$ is

$$R_{in} = V_{in} / i_i = V_{in} R_G (V_{in} - V_{out})$$

$$= R_G \left( 1 - \frac{V_{out}}{V_{in}} \right) = 10 \times 10^6 / (1 + 3.37) = 2.28 \text{M\Omega}.$$  

One will also see that the input impedance $R_{in}$ is also equal to the Miller’s input resistance, which is defined as $R_G / (1 + A_V)$, for this amplifier.

**Example 5.8**

Design the amplifier circuit shown in figure below that its transistor operates in saturation region with $I_D = 0.5 \text{mA}$ and $V_D = 3.0 \text{V}$. The enhancement-type PMOS transistor have $V_{GS(th)} = -1.0 \text{V}$ and $K = 0.5 \text{mA/V}^2$. What is the largest value of $R_D$ can have while maintaining saturation-region operation? Note that normally $R_{G1}$ and $R_{G2}$ are in M\Omega range.
Figure 5.22: A common drain amplifier

**Solution**

Using equation (5.4), which is \( I_D = K(V_{GS} - V_{GS(th)})^2 \). Substituting \( I_D = 0.5\text{mA} \), \( K = 0.5\text{mA/V}^2 \), and \( V_{GS(th)} = -1.0\text{V} \), the gate-to-source voltage \( V_{GS} \) of the PMOS shall be \( \pm 1.0\text{V} - 1.0\text{V} \), which are 0V or -2.0V.

Since the threshold voltage of the PMOS is -1.0V, therefore, its gate-to-source voltage \( V_{GS} \) should be – 2.0V.

Since gate-to-source voltage is \( V_{GS} = V_G - V_S \) then the gate voltage \( V_G \) shall be

\[
V_G = V_{GS} + V_S = -2.0\text{V} + 5.0\text{V} = 3.0\text{V}.
\]

Thus, the ratio of \( R_{G1} \) and \( R_{G2} \) shall be 2:3. Thus the value of \( R_{G1} \) And \( R_{G2} \) can be 2.0 M\( \Omega \) and 3.0 M\( \Omega \).

The resistance value of drain resistor \( R_D \) shall be \( V_D/I_D = 3.0\text{V}/0.5\text{mA} = 6.0\text{k}\Omega \).

For the PMOS to maintain in saturation mode, \( V_{SD} \geq V_{SG} - V_{SG(th)} = 2.0\text{V} - 1.0\text{V} = 1.0\text{V} \). This shall mean the drain voltage must be maintain within \( V_D \leq V_S - 1.0\text{V} \). Thus, the maximum drain voltage \( V_{D\text{max}} \) shall be \( V_S - 1.0\text{V} = 4.0\text{V} \).

Thus, the maximum value of drain resistor \( R_D = V_D/I_D = 4.0\text{V}/0.5\text{mA} = 8.0\text{k}\Omega \) for maintaining operating in saturation region.
Example 5.9
The NMOS amplifier circuit shown in figure below has Early voltage $V_M = 50.0\,\text{V}$, gate-to-source voltage $V_{GS(th)} = 0.9\,\text{V}$ and operates with drain voltage $V_D = 2.0\,\text{V}$. What is the voltage gain of this amplifier? If drain current $I_D$ is double, what will be the voltage gain?

![Figure 5.23: A drain feedback common source amplifier](image)

Solution
Let’s test to see which region the MOSFET is operating in.

\[ V_{DS} = V_{DG} + V_{GS} \]

Since gate current is very small thus, $V_{DG} = 0$ then $V_{DS} = V_{GS}$

\[ V_{DS} \geq V_{GS} - V_{GS(th)} \]

Thus, the value of LHS $> \text{ the value of RHS since } V_{DS} = V_{GS} \text{ and } V_{GS(th)} > 0\,\text{V}$. Therefore, the MOSFET operates in saturation region.

The ac equivalent circuit of this amplifier is shown in figure below.
Figure 5.24: ac circuit of drain feedback common source amplifier

From the theory discussed earlier, the voltage gain $A_V$ is $A_V = -g_m (r_o || R_L)$

The output impedance $r_o$ of the MOSFET is $r_o$ at $I_D = 500.0 \mu A$ is $V_M / I_D = 50.0V / 500.0 \mu A = 100.0k \Omega$

The drain-to-source voltage is $V_{DS} = V_{DG} + V_{GS}$. Since $V_{DG} = 0V$ and $V_S = 0V$ then the drain voltage shall be $V_D = V_{DS} = V_{GS} = 2V$.

Transconductance $g_m$ of the amplifier is

$$g_m = 2I_D / (V_{GS} - V_{GS(th)})$$
$$= 2 \times 500 \mu A / (2V - 0.9V) = 0.909mS$$

Thus the voltage gain is $A_V = -0.909mS(100\Omega || 10k\Omega) = -8.26V/V$

When $I_D$ is double to 1mA, $r_o = 50V / 1.0mA = 50.0k \Omega$

From the saturation formula, $I_D = K (V_{GS} - V_{GS(th)})^2$, the constant $K$

$$K = 500 \mu A / (2V - 0.9V)^2 = 0.413mA / V^2$$

Thus, the saturation $I_D$ formula shall be $I_D = 0.413mA / V^2 (V_{GS} - 0.9V)^2$

If $I_D = 1.0mA$ then $V_{GS} = 0.65V$ or $2.46V$. Certainly, $V_{GS}$ cannot be $0.65V$ since $V_{GS(th)}$ is $0.9V$. Thus, $V_{GS}$ shall be $2.46V$.

The transconductance $g_m$ for $V_{GS} = 2.46V$ is
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\[ g_m = \frac{2 \times 1 \text{mA}}{2.46 \text{V} - 0.9 \text{V}} = 1.28 \text{mS} \]

The voltage gain \( A_V \) when \( I_D = 1.0 \text{mA} \) is

\[ A_V = -1.28 \text{mS}(50 \text{k}\Omega || 10 \text{k}\Omega) = -10.8 \text{V/V} \]

5.6 Multistage Amplifier

MOSFET and JFET share the same ac equivalent circuit. Therefore, the way to analyse the multistage amplifier is same as the way how to analyse the multistage amplifier of the JFETs.

We shall discuss a multistage amplifier that contains both bipolar junction transistor and MOSFET device here.

Figure 5.25 shows a cascaded amplifier that contains both bipolar junction transistor and MOSFET.

![Figure 5.25: A cascoded BiMOS amplifier circuit](image)

The voltage gain of the first stage \( n \)-channel MOSFET amplifier is \(-g_m R_D\), when \( g_m \) is the transconductance that follows equation (5.6)

\[ g_m = \frac{-dI_D}{dV_{GS}} = \frac{2I_D}{V_{GS} - V_{GS(th)}} \]

However, owing to loading effect from the bipolar transistor...
junction transistor amplifier stage, the load of this amplifier shall be $R_D \| R_3 \| R_4 \| \{(\beta + 1)V_T / I_E\}$. Thus, voltage gain $A_{V1}$ of n-channel MOSFET amplifier stage shall be

$$A_{V1} = - \frac{2I_D[R_D \| R_3 \| R_4 \| \{(\beta + 1)V_T / I_E\}]}{V_{GS} - V_{GS(th)}}$$  \hspace{1cm} (5.7)

The voltage gain $A_{V2}$ of second stage is

$$A_{V2} = - \frac{\alpha R_c I_E}{V_T}$$  \hspace{1cm} (5.8)

The overall gain $A_V$ of the amplifier shall be $A_V = A_{V1} \times A_{V2}$, which is

$$A_V = \frac{2I_D[R_D \| R_3 \| R_4 \| \{(\beta + 1)V_T / I_E\} \cdot \alpha R_c I_E}{V_{GS} - V_{GS(th)}} \frac{1}{V_T}$$  \hspace{1cm} (5.9)

**Tutorials**

5.1. State the difference in terms of voltage biasing and output characteristics between a depletion-enhancement MOSFET and an enhancement MOSFET.

5.2. State the conditions for an enhancement MOSFET to operate in triode and saturation regions. Given that $I_D = 0.75 \text{ mA}$, $R_D = R_S = 5.0 \text{ k}\Omega$, and $V_{GS(th)} = 0.5 \text{ V}$. Determine the operation condition of the circuit below.
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5.3. For active load circuit below, given that $R = 15.0\,\text{k}\Omega$.

(i) What is the $I_D$ current and drain voltage $V_D$ if the active load resistance of 25kΩ is desired?
(ii) What is the gate to source voltage $V_{GS}$ for this circuit?

![Active Load Circuit Diagram]

5.4. Describe how a MOSFET can be configured as a capacitor? Given that
dielectric constant of SiO$_2$ is 3.9, permittivity in free space $\varepsilon_0 = 8.854 \times 10^{-14}\,\text{F/cm}$, $W = 200\,\mu\text{m}$, $L = 10\,\mu\text{m}$, and thickness of oxide $d_i = 100\,\text{Å}$, calculate the capacitance.

5.5. The NMOS circuit shown figure has $K = 0.5 \times 10^{-3}\,\text{A/V}^2$, threshold voltage $V_{GS(th)} = 2\,\text{V}$, $R_{G1} = 4.7\,\text{M}\Omega$, $R_{G2} = 2.2\,\text{M}\Omega$, $R_D = 2.2\,\text{k}\Omega$, and $R_S = 500\,\Omega$. Determine the values of $V_{GS}$, $I_D$, and $V_{DS}$.

![NMOS Circuit Diagram]
5.6. The common source amplifier is shown in the figure has $V_{GS(th)} = 3V$ and $K = 1mA/V^2$. Find $V_{GS}$, $I_D$, $V_D$ and the ac output voltage. If a load $R_L$ of 3.3kΩ is connected at the output what is the ac current in the load?

5.7. The depletion MOSFET shown in the circuit is required to supply the variable resistor $R_D$ with a constant current of 100.0µA. If the threshold voltage is $V_{GS} = -1.0V$. Find the range of resistor $R_D$ can have while the current through it remains constant at 100.0µA.
5.8. Calculate the ac voltage gain and output voltage of the BiMOS amplifier shown the figure.

References